1 INDUSTRY OVERVIEW

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The sweeping revolution brought about by integrated circuits has caused change not only in electronics, but also in the very act of manufacturing the integrated circuit itself. Process equipment, assembly equipment test systems, factory management systems, and process control systems have evolved right along with the integrated circuit itself. New generations of manufacturing equipment have made it possible to integrate entire systems onto a single chip. Electronic systems engineers no longer build circuits from components. Nor do they use subassemblies. Rather, the building blocks of their electronics systems are entire computer systems themselves. Semiconductor manufacturing holds the key to most electronic advancements. The ability to manufacture semiconductors affects pricing at all levels of electronics. Today's semiconductor business decision making must include manufacturing as a strategic component.

VLSI Research Inc has attempted to capture the flavor of manufacturing's importance in this series of subscription services. This section describes both the business and technical aspects of the semiconductor manufacturing. It shows how they effect and are affected by electronics and semiconductors.

Section 1.1 examines the economic relationships between electronics and semiconductors. This section provides an overview of the electronics industry's segmentation. It starts off with a brief description of the industry. It then covers market structure and dynamics. It examines the interplay between manufacturing, technology and pricing in the semiconductor market. Section 1.1 also examines semiconductor manufacturing characteristics. This subsegment starts with a description of semiconductor manufacturing. It examines the history of manufacturing and its role in shaping the future of the semiconductor industry.

Section 1.2 contains Executive Advisories centering around the overall aspects of the industry.

Section 1.3 will cover manufacturing's impact on semiconductor business decisions. It covers industry capitalization, manufacturing driving forces and provides models of different manufacturing lines. Section 1.4 will provide a place for updates to recent changes in industry structure. Both sections are unreleased at this time.

Section 1.5 gives the overall outlook and forecast for the semiconductor manufacturing industry. Section 1.9 provides a complete database for analysis of the various markets. A magnetic disk that contains the data from these tables is also included.

1.1 INTER-INDUSTRY RELATIONSHIPS

(Index continue on next page)

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(Index continue)

1.1 Inter-Industry Relationship

Semiconductors have been at the center of high technology for four decades. In recent years, few other scientific topics have drawn so much of the world's attention. Semiconductors have become of such importance that many governments around the world view them as a strategic resource. Evidence of this can be seen not only in the various government subsidies, but also in the tremendous level of espionage—both industrial and political—that occurs in Silicon Valley.

The effect of semiconductor technology on the economy is immensely complicated because so much of it occurs in a free market not subject to controls. Both demand and supply play important roles in the market. Consequently, manufacturing and technology dramatically affect the semiconductor market. Consequently, understanding the characteristics of the semiconductor market are critical in any decision making regarding manufacturing.

The purpose of this section is to show how market dynamics interrelate with manufacturing. It starts with a structural overview. It then examines the dynamics of the semiconductor market.

1.1.1 Market Structure and Segmentation

Figure 1.1.1-1 delineates the various forces shaping the industry. These forces are many-faceted, and like a long biological food chain, they begin with the general pervasiveness of electronic components. They end with penetration into totally new electronic applications. The semiconductor industry is in the middle of such a tiered economic chain containing several links. The economic chain starts with consumer purchases. This leads to new industry demand. New industry demand, in turn, spurs systems applications of electronics by industry and government. Typical applications encompass electronics in automobiles, airplanes, and military systems as well as other governmental applications, institutional uses, etc.

The chain next moves down one link to the OEM† level. This includes computer manufacturers, line-printer suppliers, test system manufacturers, et cetera. Additionally, there is another line stemming directly from consumers who purchase television sets, stereos, microwave ovens, and the like. Growth in electronic demand makes itself felt through increasing unit volume demand of semiconductors. Semiconductor sales are created as inventories become depleted.

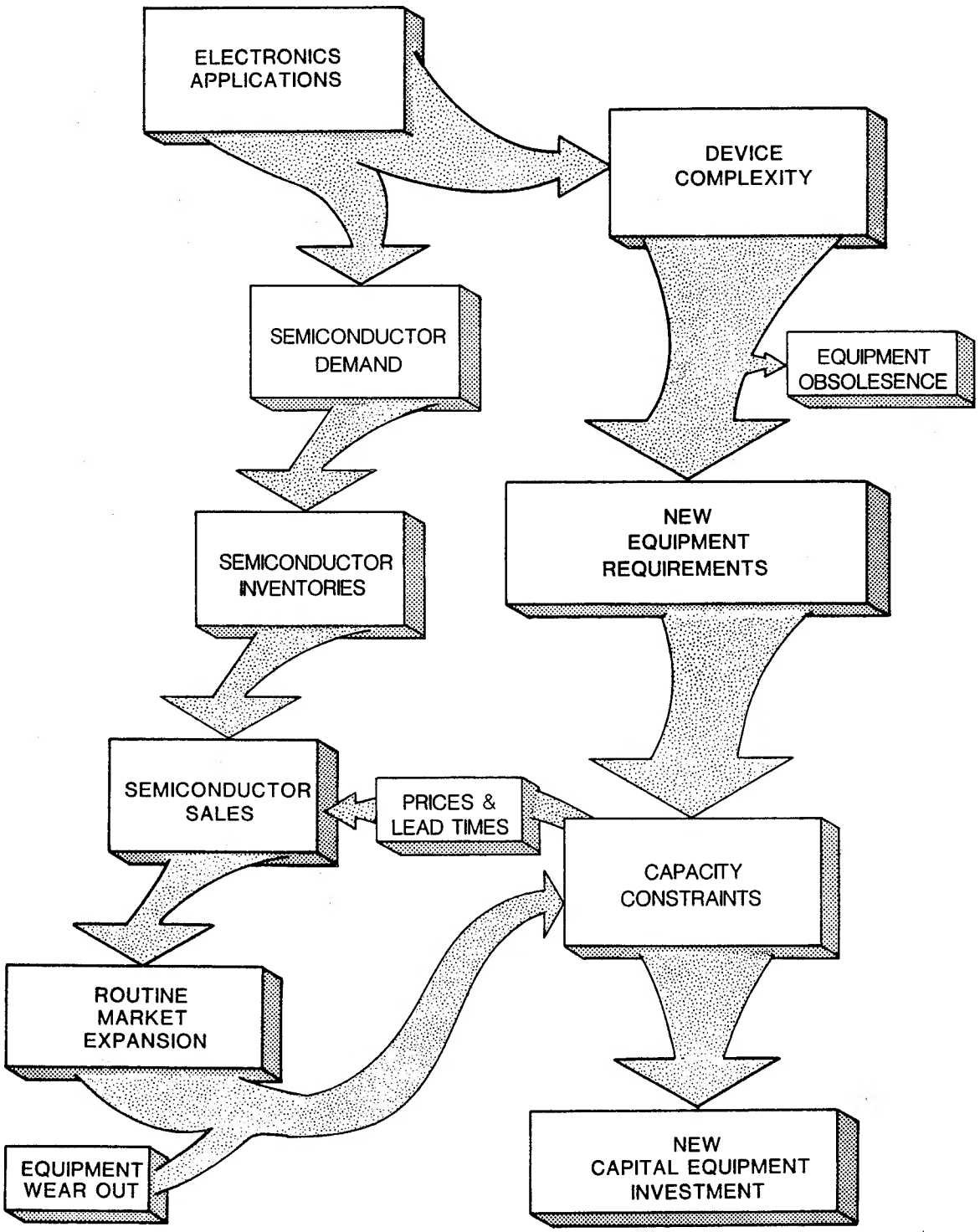
Electronics manufacturers are the sole buyers of semiconductors. Semiconductor components alone go into almost $500 billion worth of equipment that is vital to the well-being of the world. These range from things such as the high-reliability requirements of space vehicles, to the pollution-preventing control systems of automobiles. Electronic gadgets have even become the private tutors of our children with talking, spelling and teaching boxes. Along the way, these boxes have also been transformed into go-anywhere language translators, calculators, computers, games, metrical instruments and telecommunication equipment. Demand at this macro-scale makes itself felt in both new device complexity and in increased semiconductor demand.

Increases in device complexity, in turn, fragment into numerous new manufacturing thrusts, sometimes causing a kaleidoscopic appearance of new products in the manufacturing equipment market. Old equipment is made obsolete by such thrusts. New equipment is often introduced in conjunction with new semiconductor devices. This allows new devices to be both more reliably produced and more complex. For example, automotive requirements gave rise to new low temperature test methods. Voice syn-

† OEM: Original Equipment Manufacturer.

Figure 1.1.1-1

Forces Shaping
THE SEMICONDUCTOR MANUFACTURING INDUSTRY



thesis created demand for new linear test methods. Computer and office equipment needs for ever more memory have given rise to new types of semiconductor equipment which continually grow more complex. These thrusts propel semiconductor manufacturers into the purchase of ever-more-expensive equipment.

Thus there are four essential tiers to the ecosystem of the semiconductor manufacturing industry. Their relative sizes are as follows:

TIER	1987 SIZE (IN $B)
The Macroeconomy (U.S. GNP)	4498
Electronics (worldwide)	476
Semiconductors (worldwide)	44
Semiconductor Equipment (worldwide)	5

110-T1

The macroeconomy is not covered to great detail by this service. It is well covered elsewhere and so there is no need. However, Macroeconomic issues are brought into play when they are relevant to the topics of any given section. The macroeconomy is an important driver of electronics.

The value of free world electronics production is in excess of ten percent of United States GNP. Its content as a percentage of GNP has been steadily increasing. In contrast, in 1952, this ratio stood a mere two percent. There has been a steady diffusion of electronics into society for decades. Electronics have become pervasive in everyday life. This growth in applications has lead to rapid growth in electronics sales.

Electronic equipment markets are important because they are the sole consumers of semiconductors. There are nine essential segments of the electronics market. They are: Automotive, communications, computers, consumer, government, industrial, medical, office, and test and measurement. The most important of these are computers, government, communications and consumer electronics.

The computer segment is the largest electronics segment. In 1987, computer electronics production reached $134 billion worldwide. This segment includes computers, peripherals and software. The computer market has a dramatic impact on semiconductor consumption not only because of its size, but also because it follows the first derivative of the economy.

The market for computers is driven primarily by growth in worldwide industry itself. One way of measuring industry's effect on computers is through the acceleration principle of economics. That principle states that any firm's investment in new equipment will vary directly with the change of its own revenue. Thus the primary driving forces for computers will be determined by industry's magnitude of growth, not by its actual sales. Consequently, it's driven like the end of a whip—increasing or decreasing at the slightest agitation of the economy.

Government electronics is the second largest segment. Production of government electronics achieved $80 billion worldwide in 1987. Military electronics expenditures compose the majority of these sales. This segment is also one of the most stable of all electronic markets. The long term outlook in Government electronics continues to be good despite pressures from the deficit.

In 1987, communication electronics production reached $73 billion worldwide. It is the third largest electronics segment. This segment includes telephones, switching networks, PBX's and cellular radio.

The consumer segment of electronics is the fourth largest segment with sales of $60M in 1987. It is a tough market to compete in since the whims of consumer choice must always be gauged. Additionally, the product

life cycle in consumer electronics tends to rapidly escalate into maturity. Primary demand (i.e. first-time buyers) usually cause a consumer electronics product sales to explode. However, secondary demand (i.e. second-time buyers) is always much lower than primary demand. Consequently, once a primary demand peak is reached, a market soon collapses. Prices fall first, and then volume. There is a huge graveyard of here-today-gone-tomorrow consumer electronics fads. Some of these have been calculators, CB radios, and video games. Nevertheless, consumer electronics markets are important drivers of business cycles in the semiconductor market. This is because a consumer electronics market is usually at the heart of most boom bust cycles. All strong upturns have been driven by one or two hot consumer products.

While important, the other segments of electronics tend not to have as much of as effect on the semiconductor markets. Their very nature makes them track the four previously discussed markets.

The semiconductor market is centered between electronics and semiconductor equipment in the Ecosystem of VLSI. The total semiconductor market reached $44B in 1987. This amounts to 9.3% of all electronics sales. Unlike electronic content rates in GNP, semiconductor content rates in electronics have been relatively stable since 1979. Consequently, semiconductor sales will tend to grow at a rate that is roughly equal to electronics. However, as we will show later, inventory accumulation dramatically affects the business cycles of semiconductors.

There are three essential segments of the semiconductor market. They are the markets for bipolar integrated circuits (IC's), MOS integrated circuits, and discrete circuits. Each can be segmented into a multitude of smaller markets.

The market for MOS IC's is the largest. Sales of MOS IC's reached $2.2B in 1987. Bipolar IC sales accounted for $14B in sales for 1988. Sales of discretes were $8B in 1987. Further detail on the segmentation and size of the semiconductor market can be found in Section 6: Semiconductors.

Semiconductor production equipment is at the tail end of the ecosystem of VLSI. This is because semiconductor equipment is built with semiconductors and many other non-strategic components. These components sell to all industries. Therefore, they do not have a strong symbiotic attachment to the ecosystem of VLSI. In contrast, semiconductor production equipment is highly dependent on semiconductors. There are few other applications for it. Consequently, it cannot survive without a healthy semiconductor market.

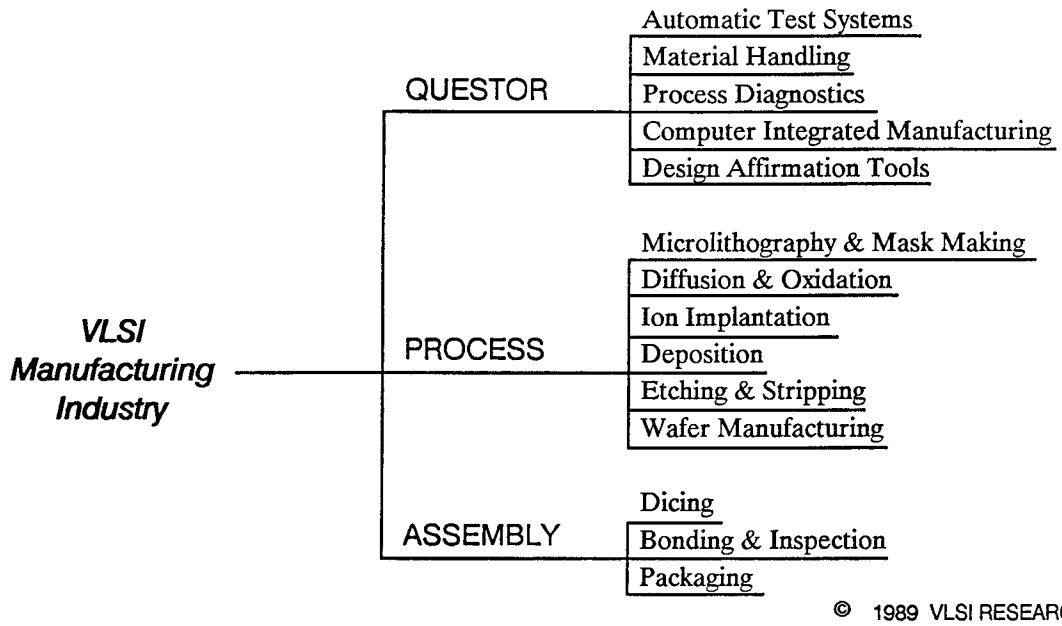
The market for semiconductor production equipment was $5B in 1987. This represents a mere one percent of all electronics sales. Nevertheless, semiconductor equipment provides a fundamental platform for the electronics industry—for without it, electronics equipment would not function for a lack of semiconductors.
There are three essential segments of the semiconductor equipment market. These are:

- Questor Systems
- Wafer Process Equipment
- Assembly Equipment

Each of the major segments shown above provide a separate and distinct
function on a semiconductor manufacturing line. Additionally, several submarkets exist within each of these four segments. A specific breakdown of questor systems, wafer process and assembly equipment is given in Figure 1.1.1-2.

Figure 1.1.1-2

SEGMENTATION OF THE VLSI MANUFACTURING INDUSTRY



Questor systems is a category created by VLSI Research to describe those systems which are used as the central nervous system of a factory. The questor systems market can be subdivided conveniently into five groups:

- Automatic Test Systems
  - ATE and burn-in
- Material Handling
  - Probers, laser repair, handlers, transport and transfer
- Process Diagnostics
  - Inspection and process monitoring
- Computer Integrated Manufacturing
  - CIM networks and software
- Design Affirmation Tools
  - Design verification and CAD interface

Further detail on each of these segments can be found in Section 3, on Questor systems.

Wafer process equipment consists of all equipment that is used in, or directly related to, the making and processing of silicon wafers. It covers all applications from growing a crystal up to wafer dicing. Wafer process equipment includes the following:

- Microlithography and Mask Making Equipment
  - Resist processing, alignment, and direct exposure
- Diffusion and Oxidation Equipment
  - Diffusion, HiPox and rapid thermal annealing
- Ion Implantation Equipment
  - Medium current, high current, and high energy systems
- Deposition Equipment
  - CVD, PVD and epitaxy

- Etching and Stripping Equipment
  - Dry etching, wet etching and cleaning
- Wafer Manufacturing Equipment
  - Crystal growing and crystal machining

Further information pertaining to wafer process equipment can be found in Section 4.

Assembly equipment consists of all equipment that is used in the mechanical process of making finished circuits. It consists of:

- Dicing Equipment
  - Sawing, scribing and dicing accessories
- Bonding and Inspection Equipment
  - Die bond, wire bond, and bonding inspection
- Packaging Equipment
  - Molding, sealing, finishing, marking and package inspection

Further information concerning assembly equipment can be found in Section 5.

1.1.2 Market Dynamics of the Semiconductor and Semiconductor Equipment Industries

The semiconductor market is well known for its market instability. An understanding of how the dynamics of the semiconductor market drive its instability helps in identifying the early warning signals of an impending shift in market conditions.

There are several key market features that play heavily in causing the industry's market instability. The four most important ones are listed below:

- Rapid growth cycles
- Sharp price fluctuations
- Rapid technical innovation
- Frequent capacity imbalances

These factors have a strong effect on the ability of companies to compete effectively. Boom-bust cycles are characterized by the entry and exit of firms into the marketplace. For example, in last cycle there was a multitude of new entrants into the Dynamic Memory Market--NMB, Micron Technology, Hyundai, and Samsung to name a few. There was also many who exited the market during the subsequent downturn. AMD, Intel, National Semiconductor, Mostek, and Motorola were among the most prominent. Matching a manufacturing strategy with a marketing strategy while maintaining the technological pace is difficult for even the best companies. However, the penalties for failure are quite severe.

These factors also have a dramatic effect on equipment companies. There is an old story that has circulated the industry for years. It goes like this: "When the economy gets a chill, electronics catches a cold, semiconductors come down with pneumonia, and the equipment industry dies." This is an apt description of how the market dynamics affects equipment suppliers.

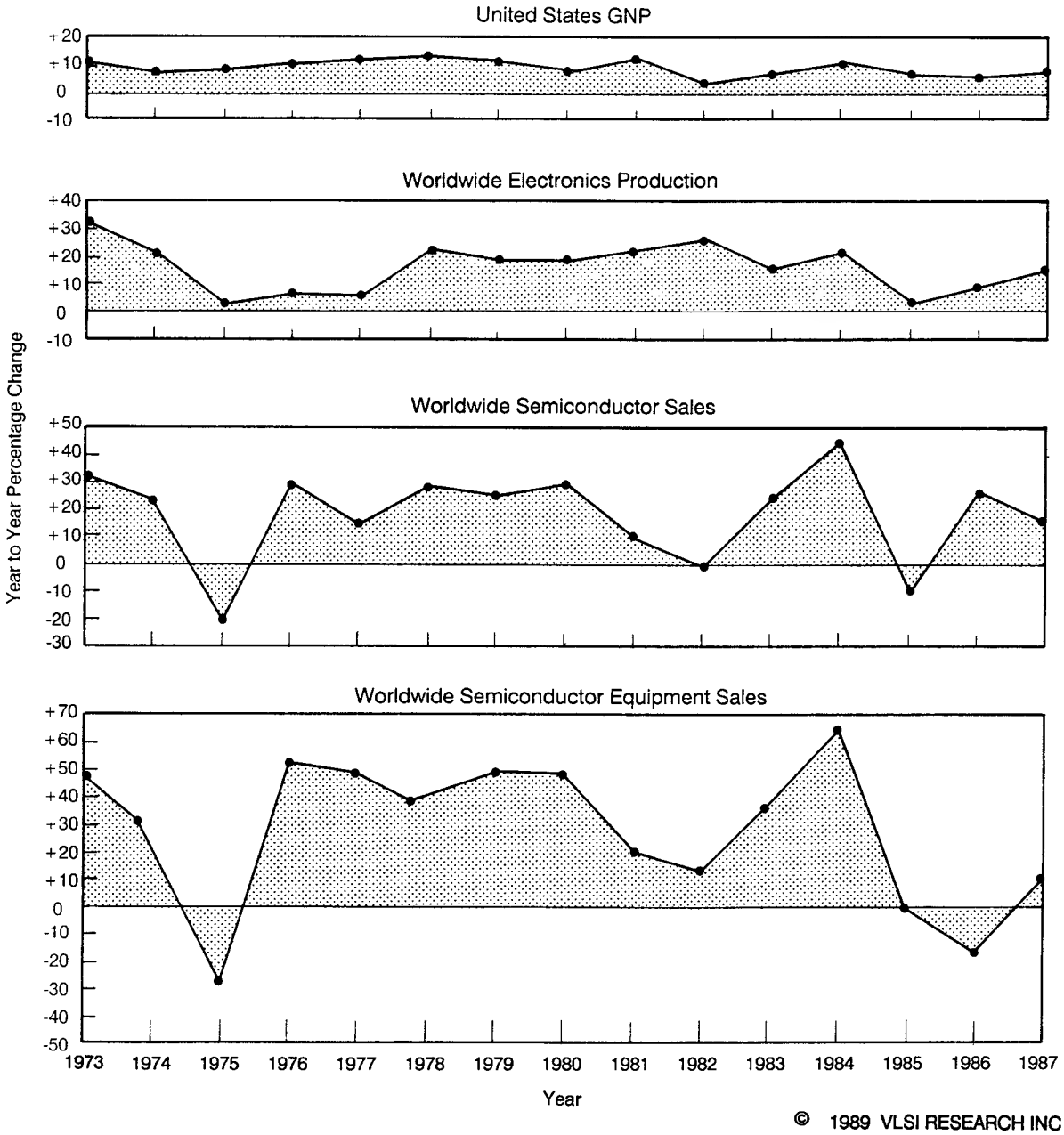
This section examines each source of instability and their affect on the VLSI manufacturing industry.

RAPID GROWTH CYCLES

The most documented characteristic of market instability in semiconductors has been its boom-bust cycles. In boom times, the semiconductor market has achieved growth rates that have exceeded forty percent. In downturns, sales have fallen by as much as twenty percent (See Table 1.1.2-1). The effect of these cycles on the semiconductor equipment market is amplified by the acceleration principle described in the contents section. Sales gyrate sharply with small changes in semiconductor growth. Equipment bookings have risen in excess of 100% in a upturn and fallen by over 95% in downturns. Managing a business under these conditions is difficult at best.

TABLE 1.1.2-1

SEMICONDUCTOR BUSINESS CYCLE
(year to year percentage changes)



The market dynamics show how these various factors interplay to cause severe boom and bust cycles in the industry as explained below:

Most upturns in the semiconductor industry have been driven by a general economic upturn. First there is an uptick in electronics. Then, each tier of the industry comes out of the downturn sequentially, creating a whiplash effect. Usually, one of two key products are behind the upturn. For example, the personal computer boom started in 1982 and peaked in 1984. It led to the most recent downturn. Prior to that, from 1976 to 1981 the industry was driven by video games and 8 bit personal computers. From 1969 to 1975, calculators and watches drove the industry.

Production in the electronics industry picks up rapidly once an upturn is underway. This causes an increase in semiconductor orders. Soon, the semiconductor industry is also well on its way to recovery. When this happens, inventories maintained by users decrease to very low levels, drawing up demand still further. The semiconductor industry soon becomes capacity limited. Shipments slow while delivery leadtimes stretch out. Longer delivery leadtimes require that electronics manufacturers keep still more inventory in order to keep their production pipelines full; further aggravating the whiplash. This effect creates a strong feedback loop that amplifies semiconductor market cycles.

Electronics manufacturers must keep a sufficient supply of semiconductors on hand to support their production needs. The supply of inventory that is needed has a direct cause-effect relationship to leadtimes. As leadtimes expand, still more inventory is needed to account for the longer delivery times. Consequently, electronics manufacturers increase purchasing activities. However, these additional purchase orders are not usually filled immediately because of semiconductor capacity limitations. This causes leadtimes to stretch out further,which in turn causes still more purchasing activity, while inventories grow to disproportionate levels. This fundamentally unstable situation feeds upon itself causing semiconductor sales to expand without limit. This effect can be seen for the most recent 1983-1984 upturn by examining the data in Table 1.1.2-2. Inventory levels are seen to have tripled between early 1983 and mid 1984, while bookings† doubled.

Invariably, this supply shortfall causes an immediate strengthening of prices. Companies already engaging in the market become immensely profitable as they ride down the learning curve. This excess profitability creates demand for more capacity. Moreover, it rapidly attracts new competitors. In the 1984 upturn, traditional suppliers such as Intel, Motorola, NEC, and TI were joined by numerous newcomers such as NMB, Hyundai, Samsung, Goldstar, Cypress, Sony, Nissan Motors, Seiko and AT&T. Even IBM made a small merchant entry. Meanwhile, semiconductor bookings, leadtimes, and inventories continued to rise.

These effects translate, in turn, into a literal explosion of sales of equipment to manufacture semiconductors. Demand for such equipment exceeds supply and so equipment backlogs also grow dramatically. Additionally, equipment manufacturers are usually somewhat reluctant to expand capacity at a rate fast enough to satisfy the industry. Consequently, equipment backlogs usually swell to unprecedented new highs in each new upturn.

†Bookings occur when a purchase order is received. It does not become a sale until the product is shipped and revenues are received by the semiconductor supplier. The lead time is the time it takes to ship an order once it is received.

TABLE 1.1.2-2

SEMICONDUCTOR INVENTORY CYCLES

(worldwide captive and merchant values in $M)

Period	SUPPLY				DEMAND	
	Sales Growth	Sales ($M)	Backlog ($M)	Bookings ($M)	User Inventories ($M)	Weeks of Inventory
83q1	6.6%	5129.7	1963.3	5488.8	4215.3	10.3
83q2	13.1%	5800.7	2195.3	6032.7	5022.6	12.1
83q3	8.8%	6309.3	2763.1	6877.1	5827.2	12.7
83q4	13.2%	7144.3	4406.3	8787.5	7380.1	15.8
84q1	3.5%	7391.0	6771.5	9756.1	8916.4	17.6
84q2	15.8%	8560.7	8654.8	10444.1	11375.2	21.4
84q3	4.4%	8940.2	8118.4	8403.8	13316.2	22.0
84q4	0.2%	8955.4	5790.0	6627.0	12741.4	17.5
85q1	-16.2%	8091.8	4009.8	6311.6	12959.8	17.5
85q2	-5.8%	7623.1	2485.2	6098.5	11586.0	16.8
85q3	-6.5%	7131.3	1058.9	5705.0	10378.6	15.5
85q4	3.0%	7346.5	765.1	7052.6	8980.3	13.3
86q1	10.1%	8260.1	1425.9	8920.9	7707.9	12.1
86q2	16.5%	9619.3	1522.1	9715.5	7564.9	11.1
86q3	5.2%	10115.6	712.8	9306.4	8118.0	11.0
86q4	-2.0%	9909.7	326.4	9513.3	8423.4	10.4

But new equipment that has just been installed does not usually become operational for about nine months. It is new, it is complex, and it is difficult to learn to operate correctly. Moreover, delivery of ordered equipment often takes another nine to fifteen months. Consequently, the overall lag between an initial market upturn and added on-line capacity will typically exceed two years. By this time, the initial cause of the upturn may have faded.

Two dramatic time-displacement effects take place as a result: First, the semiconductor manufacturer, observing this demand upon his already limited capacity comes under great pressure to buy still more equipment, for he is observing the effect of equipment purchases which occurred some two years earlier. His objective will be to get in equipment as quickly as possible.

Secondly, at the same time, the supplier will be booking equipment planned for delivery one to two years in the future. So the suppliers vantage point is two years into the future. This creates a perceived discrepancy of about four years between that of the seller and that of the buyer. This displacement between booking, delivery and increased capacity, causes the buildup of a pressure front between supply and demand. Anticipatory effects result and they often come to dominate.

Eventually, three events occur and usually in unison:

- Semiconductor equipment manufacturers' bookings catch up with real demand levels.
- Electronic demand softens.
- New semiconductor capacity comes on-line to satisfy order levels.

Excess orders cause equipment manufacturers to build equipment at significantly higher rates. For example, semiconductor capital equipment shipments grew by 39.3% in 1983 and then by 64.7% in 1984. The problem facing semiconductor equipment suppliers in 1985 was quite simple: Two years worth of capital equipment had been shipped in 1984. Semiconductor capacity grew rapidly as a result. By the end of 1984, MOS semiconductor production capacity was 83% higher than total demand dictated. Semiconductor manufacturers soon caught up to the real level of electronics demand (i.e. that level of demand that does not include excess inventory, orders, or backlogs).

Semiconductor shipments expand rapidly as new capacity comes on-line. Growth quickly exceeds demand. In 1984, semiconductor sales grew by 44%. One tier up, overall electronics sales grew by 21%. This was much higher than needed. Eventually, component leadtimes started to fall and inventory requirements fell also. The overall effect reversed and anticipatory effects again came to dominate as the industry stalled. When electronic demand softens, it will often trigger an industry downturn. The effect that these cycles have upon prices is dramatic, as will be seen in the following text.

MARKET PRICING

There has been a long history of rapid price movements in semiconductors. Prices typically fall over the long term as Table 1.1.2-3 shows. When a new product is introduced, prices are usually quite high. A range of $70 to as much as $300 is typical depending on supply conditions.

The price of state-of-the-art chips hasn't varied greatly over the years. In the early 1950's, the first transistors sold for around $70. In 1969, an Intel 1101 sold for $65 in lots of 100. In 1979, 64K DRAM's were selling for $128. In mid 1980, an Oki 16 kilobit static RAM was selling for $72 in lots of 100 to 999. In 1986, 1 megabit D-RAM's were selling for $51. Consequent-

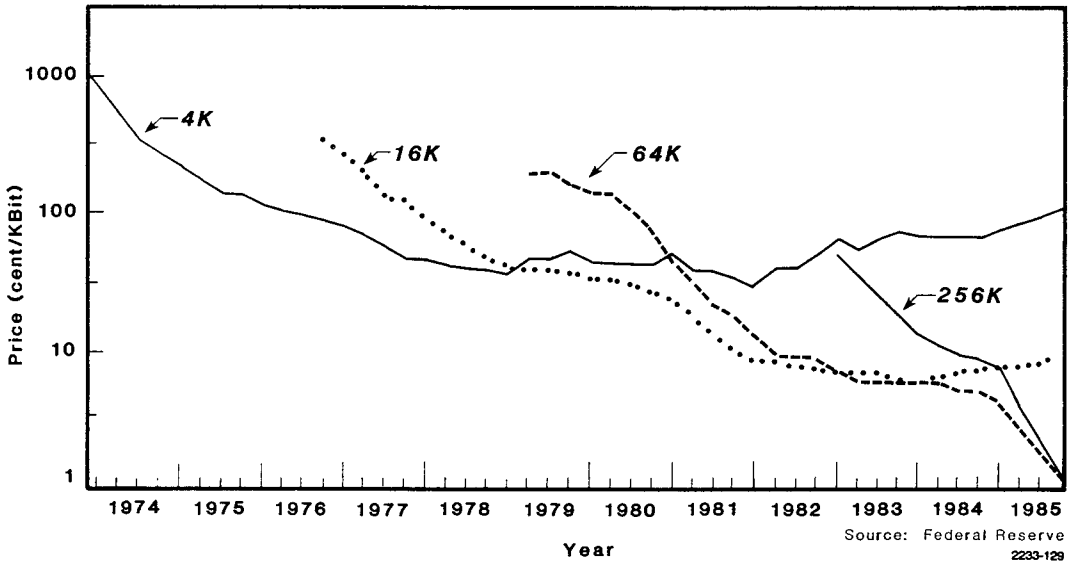


TABLE 1.1.2-3

PRICE TRENDS IN DRAM's

ly, the range of prices for newly marketed units have changed little. However, prices can be quite high when market conditions are in short supply. For example, in 1988, Intel 386, 32 bit microprocessors have sold for around $300.

Nevertheless, the individual price of a specific product will usually drop quite rapidly following its introduction—usually down to about $10 to $20. As the component matures, its price will settle further, down into a $5-$10 range. Upon reaching maturity, it will typically cost between $2 and $4. The part will maintain this $2-$4 price range until it becomes a commodity item, after which its price trails down to below $1. As the device matures, there is often a collapse in prices. This is particularly true in DRAM's as the following example shows:

By the springtime of 1984, it had become clear that the semiconductor industry was over installing 64K bit DRAM capacity and that by year's end there would be enormous excess capacity. At the time, such parts were typically selling for between four and five dollars each. Manufacturing costs were just over $1.00. This was attracting many new entrants and lots of capacity building. As the capacity began to come on-line a wave of cutthroat pricing drops ensued.

By October, Micron Technology had dropped its 64K bit DRAM prices to $1.85—well below the commodity price line of $3.00. By December, Japanese prices had dropped to $1.95 (¥480). Also by December, buyers of 64K bit DRAM's who had previously stocked up heavily in the spring at prices of $5.00 each began unloading their unused quantities at the newer prices. By the middle of 1985, prices were as low as 30 cents. That represents a compounded monthly decline of 14 percent!

Capacity shortages have the opposite effect and can bring rapid price rises. This effect was exhibited recently in 1987 when a combination of low semiconductor inventories and a sudden increase in electronics sales created a surge in semiconductor demand. Nevertheless, two years of low capital in-

vestments had left the semiconductor industry without enough capacity. This occurred with computer products in particular, as companies waited on 1M bit DRAM's and 32 bit microprocessors. Sun, IBM, Attain and Apple all noted problems with shipments due to semiconductor shortages. High demand coupled with low inventories yielded inflated semiconductor prices. Average selling price of all IC's rose by 19.3% between January and December of 1987. Price pressure was most intense later in the year. IC prices rose at a 191% annual rate in December over November. 32 bit microprocessor prices rose to in excess of $300. DRAM prices increased at a 374% annual inflation rate for 256K bit versions. Prices for 256K bit DRAM's rose from $2.40 in June 1987 to $10.00 by May 1988. One megabit prices rose at a 75% annual inflation rate from $18.00 in June 1987 to $30.00 by May of 1988.

One might think that these price variations are purely market related and thus random. However, they have had a periodicity of approximately five years. Price collapses have occurred in 1974, 1981, and 1985. Shortages have occurred in 1973, 1977, 1984, and 1987. Market conditions do play an important role. However, lead-lag relationships in capacity building play a more significant role in creating disequilibrium† in these markets.

The pricing history of DRAM's indicates a market in which demand is highly elastic in the *long run* over several years. The continuous decrease in price per bit over time and the subsequent explosion in memory demand is proof of this. In fact, the specific *long-run* price elasticity demand for DRAM bits is 6958, as based on measurements between 1977 and 1984. Hence, demand increases by almost seven thousand bits for a one cent drop in Kbit prices. An elasticity number greater than one is considered elastic. Consequently, *long-run* price elasticity of demand for DRAM's is extremely elastic.

However, the history of price collapes indicates that *short-run* demand for semiconductors is highly inelastic. The sharp fluctuations in price over six month periods is strong evidence of this. Such inelasticity occurs because price drops are not readily translated into new demand for devices. Most electronics markets are not very price competitive, so cost reductions are not immediately translated into lower equipment prices. Moreover, it takes time to design semiconductors into new applications which could bring about new demand for greater volume. The result is that demand for semiconductors does not respond quickly to price change. This aggravates price fluctuations and makes the market price inelastic in the short run.

This short run inelasticity can be demonstrated by examining the 64K DRAM market during the 1984 to 1985 period. As prices fell in 1985, unit volumes didn't skyrocket as might be expected in an elastic market. Rather, it stayed reasonably constant. This clearly indicates an inelastic market†. The specific short-run price elasticity of demand was measured for 64K DRAM's in 1985. It was found to be 0.083. In plain English, that meant that for every additional 89M units produced in 1985, prices dropped by one dollar. This impact of this was that every additional fab module brought on line in 1985 reduced the absolute size of the DRAM market by $545M!

As can be seen, this price instability is very sensitive to capacity changes. It is also very sensitive to technical innovation. Semiconductor prices tend to be capacity driven in the short run and technology driven in the long run.

† Disequilibrium is a term used by economists to describe an imbalance between supply and demand. Disequilibrium in a market results in unstable prices.

† The opposite example occurred in late 1987 with 256Kb DRAM's. Prices skyrocketed. By mid-88 prices were almost four times late '87 prices. Yet, unit volumes were *increasing*. This is clearly an inelastic market in the short run.

TECHNICAL INNOVATION

Technical innovation affects semiconductor market dynamics in two ways. The first is through new device technology. The second is through the learning curve.
The onset of a new generation of device technology can be a triggering mechanism that initiates a price collapse. Demand for an old generation falls off rapidly when a new generation becomes available.

Often, semiconductor manufacturers will find themselves in a crushing vice of economic forces. Their new capacity for current generation parts is finally coming on-line. However, the next generation is already in pilot production. Customers are anxiously awaiting the new generation part. Once word of its imminent production gets out, demand for the current generation quickly falls off. Sagging demand and new capacity causes a price collapse. Losses will begin to steadily mount during this time. This is a most critical point in time. For a manufacturer must expand capacity for the new generation part. Its existing production facilities are obsolete. The last thing that a company wants to do under these conditions is invest more in DRAM's. Those that succumb to this urge and don't make the investments eventually fail. Those that do, will have the capacity to reap extremely profitable years in the next capacity shortage.

New technology and failure to invest eventually creates a technology shortage. For example, it only cost about $1.00 to manufacture and sell a 64K DRAM in 1984. The most efficient plants could sell at a break-even price of 87 cents. The least efficient were in the $1.30 range. At an average price of $4.48, the net pretax profits were $3.48 per device. It cost $10.91 for an efficient plant to build a 1 megabit DRAM in early 1988. This translates into pretax profits of $19.09 per part at a selling price of $30.00. Note, these are pretax margins in excess of 60%!

This is why so many companies find the DRAM market so attractive. This is especially true of new market entrants who have not experienced the downside risk of a price collapse. The reasons for failure is usually blamed on a company's management, not the market. Consequently, there is always a group of new market entrants anxiously awaiting the next upturn.

The learning curve has a well documented, long-term effect on semiconductor prices. The learning curve is simply the long-term erosion of manufacturing cost as a result of production experience, design shrinks, and yield increases. Costs decline as more devices are produced. There are numerous technical driving forces which drive the learning curve. These forces are discussed in more detail in Section 1.1.3 and in Section 1.2.

It should be pointed out that the learning curve is not market driven, it is technology driven. Consequently, it cannot be measured by examining semiconductor prices. This is a common mistake made by most analysts of the semiconductor market. Price instability due to market dynamics make it difficult to sort out both effects. Thus, learning curve economies can only be measured in terms of real manufacturing cost.

MARKET SUPPLY

Capacity imbalances are the most important feature of market supply dynamics in the semiconductor market. These capacity imbalances are caused by the time lag in which it takes to install capacity and to dissipate it when there is an excess. There is a 24 to 28 month time lag between when a decision to add capacity occurs and the point in time that it becomes fully operational. Hence, a decision to add capacity will not increase supply into the marketplace for over two-and-a-half years. Consequently, capacity shortages can not be readily alleviated by capacity expansion. Hence,

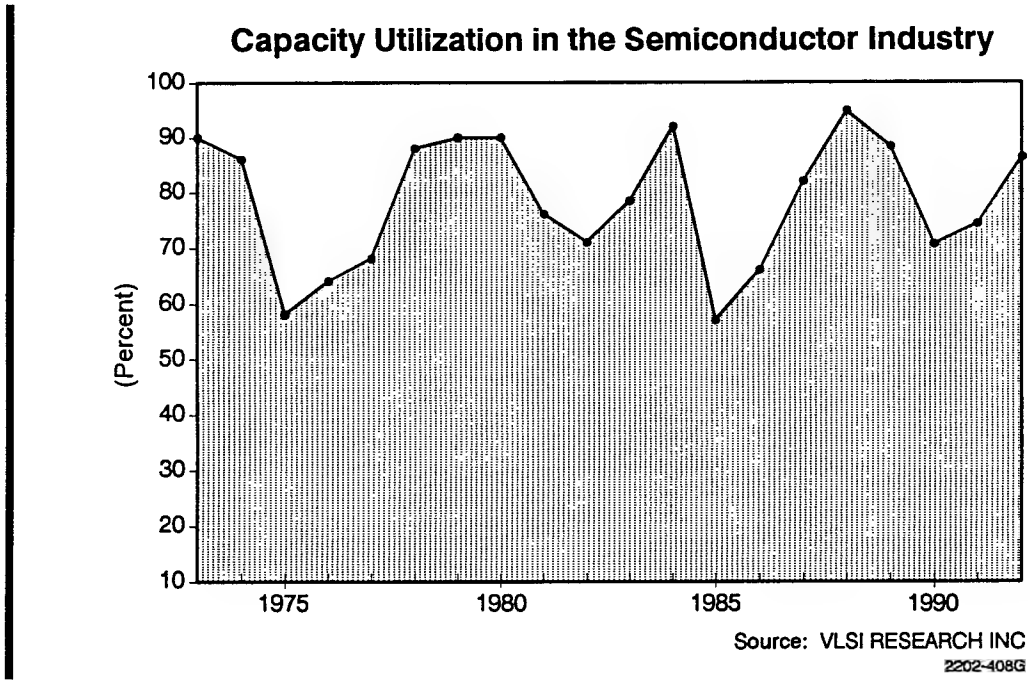
prices will continue to rise, generating excess profits. This attracts new competition. It is very easy to generate excess capacity two years into the future when this occurs. Decisions to add capacity are made all around the globe at approximately the same time. This capacity invariably comes on-line simultaneously. A domino effect of falling prices occurs as each new fab comes on-line. The resulting excess capacity shuts down investment for another two to three years. New technology will then create a new shortage.

As a result, capacity utilization for the semiconductor industry varies greatly over time. It can be seen from Figure 1.1.2-4 that it takes roughly two-and-one-half years to work off excess capacity. This is a key factor in driving the five year price cycle discussed earlier. It has typically risen to an excess of 90% during boom-times. It has fallen to as low as 58% in bust-times. Moreover, extremely hot markets can create a tremendous level of excess capacity. In 1985, there was a total demand for 13 DRAM factories in the world. Yet there were over 60 DRAM plants that were either on-line or in various stages of construction. Japan alone started eleven plants in 1984 and twenty-one plants in 1985. DRAM capacity utilization fell below 20% in 1985 as new plants continued to come on-line. This aberration is clearly the result of this five year cycle.

1.1.3 Economic Models of the Semiconductor Industry

This section applies economic theory to semiconductor market dynamics. Its purpose is to provide economic models which add insight into how and why the various market characteristics interact to cause disequilibrium in the semiconductor market. Three models are discussed in this section. They are: Learning Curve Economies, The Forward Sloping Supply Curve, and Cochranes Theorem.

Figure 1.1.2-4



LEARNING CURVE ECONOMIES

The Learning Curve has played a critical role in driving the rapid growth of semiconductor usage in electronics as was mentioned in Section 1.1.2. It was the semiconductor industry that first discovered, and applied learning curve economies. Learning economies occur as production increases and a plant becomes more efficient. As production experience is gained, a company literally learns how to make a product better; it's designs are improved; die sizes are shrunk; and it's process gets debugged. Consequently, wafer fab yields rise and even assembly yields rise. As yields rise, more product is shipped per unit of cost. Thus, revenues rise while total manufacturing costs stay constant. Average manufacturing cost per device declines.

Learning curve economies provide an important strategic advantage to the first company to enter a new market. The sooner a company enters a market, the quicker will be it's gains from being first to ride down the learning curve. Therefore, the first company to enter a market will always have a manufacturing cost advantage—in theory. The company must first be an efficient producer for this strategy to work. Otherwise, the comparative advantage provided by the learning curve will not offset the disadvantage of higher overall manufacturing costs.

It was Thomas Hinkelman at Fairchild who first developed the strategy of using the learning curve to continually lower prices. This development in the mid-sixties allowed Fairchild to have a strong profit advantage while it eroded the profitability of it's competitors. Moreover, lowering price caused the early IC market to blossom.

There are three factors that are essential to a viable learning curve strategy. First, it is essential to have a strength in component design. The first to design a new product is the first on the learning curve. Second, a top notch sales and marketing ability is also essential. A sales and marketing expertise allows a company to quickly build the sales volume to get down the first part of the learning curve. A company must be able to quickly get customers to 'design-in' a new device into their electronic equipment. Moreover, customer needs must be well understood in order to gain information about future device design requirements. Third, an expertise in manufacturing is needed. This allows a company to maintain its learning curve advantage over time. An example of how important these three strengths are can be seen in the competitive market structure that ensued after the first 'Fairchild brain drain'. The so-called brain drain occurred in the late sixties when most of Fairchild's key talent left. Robert Noyce and Gordon Moore left to form Intel. With them, went most of Fairchild's design talent. Jerry Sanders left to form AMD. With Jerry, went Fairchild's sales and marketing expertise. Charles Spork left to join National Semiconductor. With Charles, went Fairchild's manufacturing strength. A unique market structure emerged in the early seventies as a result.

Intel, having the design strength, was usually the first to enter a new market. The most important semiconductor innovations of the seventies emerged from Intel. Inventions such as the microprocessor and the Dynamic RAM impacted everyday life. Intel was also the most profitable of these three silicon valley companies.

AMD, would soon follow Intel into a market with its own version of the technology. AMD would often offer variations of the device that allowed it to win design-ins away from Intel. AMD eventually would catch-up and pass Intel on the learning curve. Consequently, AMD was also highly profitable in the seventies.

By this time, National Semiconductor would be entering the market. It's manufacturing prowess allowed it to immediately enter with a manufacturing cost advantage. Intel would soon exit the market for more fertile grounds with a new device generation. AMD would also eventually exit. This

would leave only National. Today, National Semiconductor still profitably produces many parts for markets that it captured in the seventies. It is manufacturing prowess that has allowed this. This prowess has even lead to the humiliation of some Japanese companies. In the early eighties, a joint venture with OKI lead to National's building 64 DRAM's in it's Utah facilities. National consistently out-yielded and out-costed OKI's best plant by a margin that exceeded ten percent. OKI's engineers were dismayed.

The competitive aspects of learning curve pricing cannot be ignored. There is a fragmentation of competition that occurs after a device has been introduced. Market concentration ratios display this, as shown in Figure 1.1.3-1. The first firm into a market has a monopoly and prices accordingly. Once a few firms have entered the market it will resemble an oligopoly. Prices remain high because the industry is still capacity limited at this point. A semiconductor manufacturer might charge $70 for a part that costs only $10 to make. However, once several competitors have entered the market for a particular part number, it will resemble a purely competitive market, and prices fall accordingly as more capacity comes on-line.

Once several companies have entered the market no one has control over pricing. Prices fall to cost plus a reasonable profit. The market becomes a model of pure competition. The product is virtually homogenous with the exception that the producer's name is on it. However, this is more a legal formality. Pull the cover off a computer and one can often find the same part numbers from several different producers on the PC boards. Buyers seldom have brand preferences. There is also complete freedom of entry for existing firms into new product markets. This is especially true for commodity products such a DRAM's. Product development costs are not that high as Table 1.1.3-2 shows.

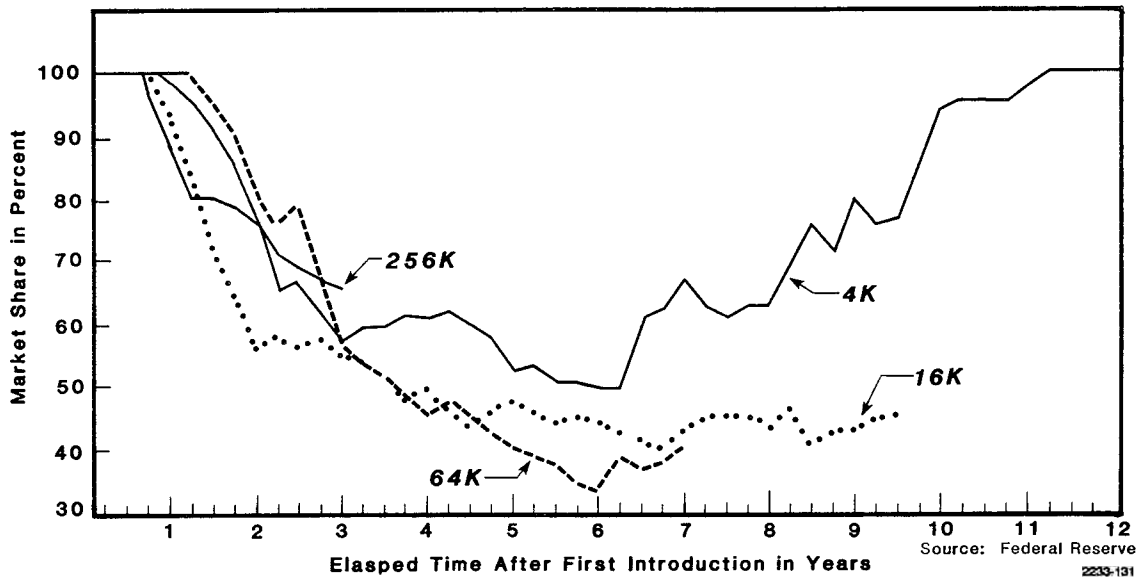


TABLE 1.1.3-1

DRAM MARKET CONCENTRATION RATIOS

(total market share for top 3 competitors)

TABLE 1.1.3-2

DRAM PRODUCT DEVELOPMENT COST
(in $M)

R,D&E Cost	*1K*	*4K*	*16K*	*64K*	*256K*	*1M*	*4M*
Design	0.06	0.2	0.4	0.8	0.2	0.4	0.7
Product Engineering	0.12	0.4	0.8	3.2	0.4	0.8	1.4
Process Engineering	0.07	0.5	2.1	8.2	1.7	6.4	24.0
TOTAL	0.25	1.1	3.3	12.2	2.3	7.6	26.1

For those products with high development costs, a company can simply 'reverse engineer' another company's products. Process technology is usually available through equipment suppliers. There is also an abundant supply of venture capital to fund new start-up companies. Information about the market is easily obtained and advertising for existing product lines is rare. Advertising is usually limited to new product lines or image ads. Moreover, there has been no government intervention as with agriculture. Consequently, learning curve pricing is merely the competitive response to a market that is in transition from a monopoly to pure competition.

The difference between the learning curve as measured by cost and the learning curve is shown in Figure 1.1.3-3. It shows both price and total cost for 64K bit DRAM's over an eight year period. Profits are high during the early period of a market. They were above 70% for 64K bit DRAM's in the first year of the market.

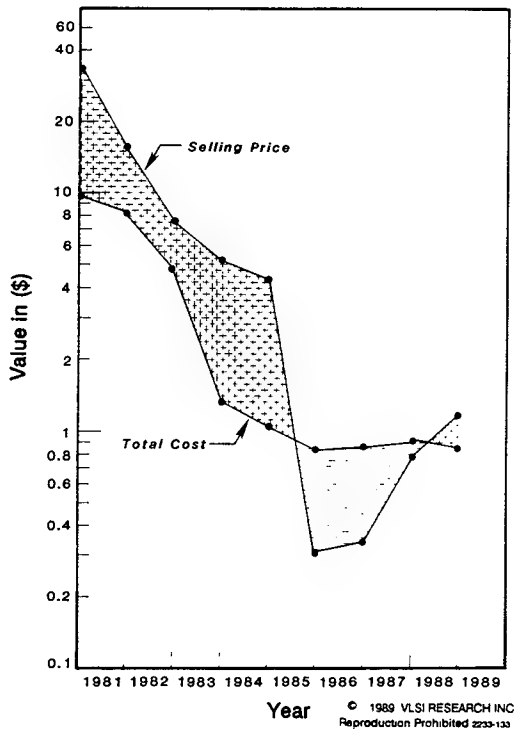


Figure 1.1.3-3

PRICE VERSUS COST FOR 64K BIT DRAM's

These high profits in the early years of a device generation are a result of the early monopoly of the first entrant, a shortage of manufacturing capacity and the short term device inelasticity of the market. However, prices do fall with cost after competition heats up. Price fell at a greater rate than cost for the first two years of the market life cycle for 64K bit DRAM's. This was during a period of excess capacity—1981 and 1982. Concentration ratios also fell rapidly during this period. Several Japanese companies entered the market after Texas Instruments and Motorola pioneered it. However, capacity shortages in 1983 and 1984 lead to excess profits. It can be concluded that learning curve economies do occur. However, whether or not this translates onto lower prices depends upon the pressure of increased competition and capacity conditions. It is doubtful if prices would be reduced if there were a lack of competition.

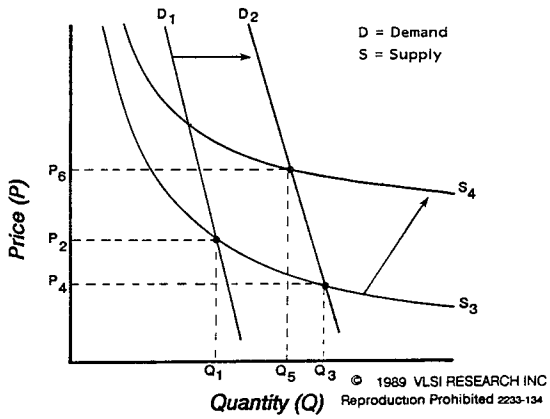


Figure 1.1.3-4

The Forward-Sloping Supply Curve of Semiconductors

THE FORWARD SLOPING DEMAND CURVE

The theory of a forward sloping demand curve was first developed by VLSI Research to explain the unique interaction between supply and demand in the semiconductor market. The combination of increasing demand and learning-curve cost declines cause semiconductor producers to produce ever larger quantities of products at ever decreasing prices. This effect creates a supply curve that slopes forward, as depicted in Figure 1.1.3-4. Such a forward-sloping supply curve foretells a fundamental instability in a market. Prices will continually fall while quantities demanded will rise in such an environment. This unique situation has provided the strong long term growth of the semiconductor industry. The effect will start when prices reach the point P_2 on the curve at production quantities of Q_1. Costs decline as the semiconductor industry rides the learning curve down to production quantities at point Q_3. This allows a price drop from P_2 to P_4, as demand increases from D_1 to D_2. Semiconductor revenues will diminish as prices trend downwards. The semiconductor manufacturer will be prompted to introduce more new devices which will have improved capability. These new devices will be on a higher supply curve, S_4 and will command higher prices (P_6) at similar quantities (Q_5). However, real prices as measured in price per bit are actually lower. Thus, a new product life cycle will be generated. Demand for newly designed parts will become far greater when its prices reach parity with the old part. Hence, rapid growth in the semiconductor market is assured by the nature of the supply curve. In the long run, demand is highly elastic. It grows constantly because real prices are constantly falling. The slope of the supply curve is dependent on the industry's learning curve.

COCHRANE'S THEOREM

Cochrane's Theorem was originally developed to describe the impact of technology on agriculture. There are several parallels between semiconductors and agriculture that make this model valid. Semiconductors were once described as being "the crude oil of industry in the 80's" by Jerry Sanders, Chairman & CEO of AMD. This statement implies that the semiconductor industry of the 80's will reflect prosperity similar to that

of the OPEC countries of the seventies. Semiconductors are a commodity item much like crude oil. However, there has been no cartel to support prices.

Instead, the semiconductor market appears to be much more like the classic agricultural markets—for example, grade A red winter wheat. Some Japanese executives even call it "the rice of industry." Like agriculture, mature semiconductor markets are almost textbook examples of pure competition.

Another aspect of the semiconductor market which is similar to agriculture is the manufacturing process. There are high capital costs in this market and these have grown at rapid rates just like in farming in recent years. Fixed costs are high, and most variable costs are nonrecoverable once the process has been started. Materials, labor and capital must all be invested to make the wafer. There are no guarantees that this wafer will be good. The semiconductor manufacturer must 'sow' its silicon, investing most of its money up front. Only later can a crop be yielded. Profitability is dependent on the absence of a 'rain' of particles onto the wafer.

Moreover, the classic problems of oversupply in agriculture is also abundant in the semiconductor market. In agriculture, the problem of oversupply has been aggravated by a high degree of fixed assets, inelastic demand, low income elasticity, rapid technological change, and competitive structure.[†]

To see the comparison, look at these parallels between semiconductors and farming as drawn from W. W. Cochrane's 1958 textbook, 'Farm Prices, Myth and Reality'.

In this book, Cochrane explains a shift in the supply curve as being due to increasingly greater farm output occurring in combination with technological advancement. As new output-increasing technologies become available, they are adopted without changing any of the fundamental input variables such as plant and land. Moreover, the competitive structure of the agricultural industry accounts for a continued acceptance of output-increasing technology. He argues that this is typical of an inelastic market.

Cochrane's theory is clearly synonymous with what has taken place in the semiconductor industry. As more companies have entered the industry, competitiveness has grown keener. In order to remain competitive, all companies have been forced to adopt increasingly complex technologies. The next question then becomes: how does the market react to these increases?

Both agriculture and semiconductor products are considered to be "generic" in the market place. Any one company's product can be substituted with that from any other. Therefore, product pricing becomes dependent upon market price. Market price, in turn, is dependent upon supply and demand. For example, if supply is less than demand, market prices will tend to be high. According to Cochrane, the only way for increasing income in this type of market is to adopt a cost-reducing technology. But the technology itself is output-increasing. So, prices fall anyway. This causes a catch-22 situation for those not using the new technology. If they do not purchase the new technology, they will be squeezed out of the market. If they can afford the equipment, they will optimize output, thereby further forcing down the price of the commodity. In other words—The average farmer of the period was on a treadmill with respect to technological advancements.

When prices dropped, farmers stayed in business even though they were losing money on total cost. Prices were below average total cost, but above average variable cost. The salvage value of assets is low. Consequently, the most profitable position is to stay in business and expand capacity. Next season, farmers would dou-

[†] Dale E. Hathaway, "The Agricultural Treadmill," Government and Agriculture, New York: Macmillan, 1963, pp. 107-130.

ble-up rows of planting and use more resources, each thinking that increasing production would increase last year's sales. Since supply increased rapidly but demand stayed constant, prices collapsed.

Similar conditions exist in the semiconductor market. Demand is inelastic in the short run. The result of this inelasticity is that prices drop rapidly once several competitors enter the market. The presence of several competitors creates a state of oversupply. Competitors respond by reducing die size. This increases production and lowers cost since more good dice can be made from the same area of silicon which costs no more to produce. Moreover, fixed assets are more rapidly amortized. Supply increases but demand stays constant and so prices drop. Income increases since production rises faster than the drop in prices. The cycle repeats itself over and over. The market is in continuous disequilibrium.

Notice that there is one important difference between semiconductors and agriculture. Semiconductors have a high degree of income elasticity which aggravates supply by spurring an excess of entrants into the market during good times.

We all witnessed the effects as American farming went from small farms to giant land management corporations. Many of us in high-technology are first-generation graduates from those farms. And this change in farming was propelled by technology—just like in the semiconductor industry. Small companies simply cannot afford to build huge DRAM plants. The current capital cost of a $300M plant is well beyond their reach. Venture capitalists can't afford to fund this. Moreover, even the major Japanese corporations are finding it difficult to stay in this market. They're quickly moving to microprocessors and ASIC's. Consequently, today's commodity semiconductor market is rapidly evolving into the political preserves of a few nations.

1.1.4 New Strategic Thrusts in the Semiconductor Industry

There are several new strategic thrusts that companies are now taking to avoid the perils of commodity semiconductor markets. Most new strategies are directed at either avoiding commodity markets altogether, or at controlling them. A third, less popular strategy, is a rationalization of competition through vertical integration. American strategies have focused on both vertical integration and the avoidance of commodity markets. Japanese strategies have focused on controlling commodity markets by restricting supply.

Figure 1.1.4-1 provides a strategic placement table for semiconductor companies. The X-axis shows the share that niche products hold of a company's total manufacturing. The higher the percentage, the lower its participation in commodity markets. The Y-axis shows captive usage of semiconductor manufacturing for a company's own electronics products. This is a measure of vertical integration. Those pursuing a niche market strategy drive their company's toward the right-hand side of the figure. A commodity supplier moves to the left-hand side of the figure. Vertical integration strategies are pursued by moving vertically on the figure. A high degree of vertical integration is depicted by companies in the upper left-hand box. Captive companies must be very highly integrated in order to justify in-house production of commodity semiconductors.

Niche market strategies are pursued by addressing small value added portions of a commodity market. Products are typically differentiated with new technology. For example, the ASIC market was niched out of the TTL gate market. It allowed customers to integrate whole boards of TTL gates into single chips. This made end-use products smaller, more reliable and less expensive.

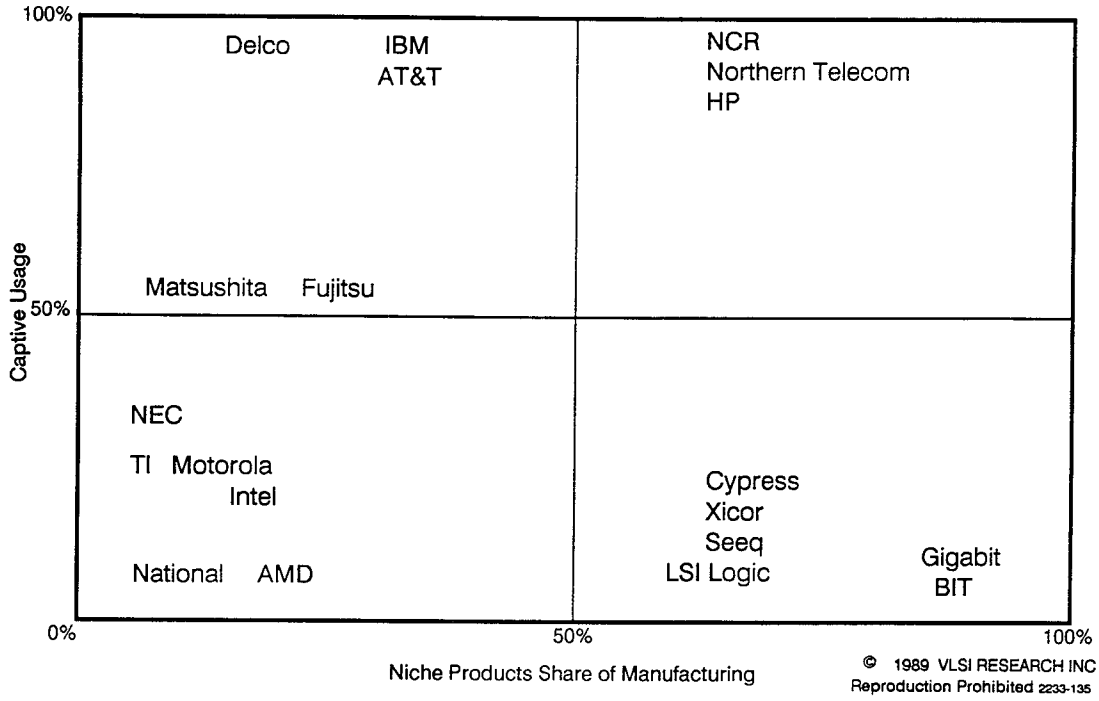


Figure 1.1.4-1

STRATEGIC PLACEMENT IN THE SEMICONDUCTOR INDUSTRY

A niche market can be an ASIC, a High Speed Static Memory, VRAMs, a special Telecom part, etc. These markets are usually hard to identify; they are rarely covered in publicly available market research; and they are typically below $100M in size. If they grow much larger they become commodity markets.

The small size of niche markets make it difficult for companies with commodity manufacturing strategies to address. One reason is that their plants are too finely tuned to producing a few products. Plant-wide efficiency drops when multiple products are introduced on the manufacturing floor. Thus, overall manufacturing costs rise. Such a company will lose its ability to compete in commodity markets if it tries to address niche markets. This efficiency loss protects the smaller producer. Niche market customers are willing to pay for inefficient production because a new technology will add value to their electronic product. Learning curve economies do not play a role in niche markets since production levels are so small. This adds further protection for the small producer.

Success in niche semiconductor markets is determined largely by a company's ability to quickly turn-around new designs and to quickly achieve production yields. There is no time to slowly provide incremental improvements to a slowly evolving process. A company must yield the first wafer and every wafer thereafter. Consequently, these markets favor small American companies. These market characteristics have made it possible for many American companies to succeed against the best world-class competition.

Vertical integration has proved to be a viable strategy in Europe, Japan and among the United States captives. It works best among those electronics companies that have established their own semiconductor organizations. Few, if any, acquisitions of a semiconductor company have worked. Most

such acquisitions have been marked by promises of great market leverage due to the virtues of vertical integration. However, the results of these acquisitions have generally been dismal. None have brought any market leverage due to vertical integration. Honeywell/Synertek, GE/Intersil, IBM/Intel, Exxon/Zilog, Gould/AMI, Schlumberger/Fairchild, and United Technologies-/Mostek have all failed to some extent. Some have been spectacular disasters.

Schlumberger bought Fairchild for $456M in 1979. They then spent over $1.5B to renovate the company. Yet, it has continued to lose money. After spending well over $2B, they finally gave up and sold Fairchild to National Semiconductor for a mere $122M in 1987. United Technologies sunk over $1B into Mostek before selling it to Thomson-CSF for a reported amount of $60M. Even IBM eventually backed out of their partial purchase of Intel.

Few attempts at integrating upwards have been successful. Intel has been the only merchant semiconductor company to successfully build an electronics division that consumes its own products.

A third strategy involves controlling the instability of commodity semiconductor markets by restricting supply. This was first attempted by MITI after Japan's failure to meet the terms of the Semiconductor Trade Agreement of 1986. Japan had originally tried to control prices by simply raising to the Fair Market Values (FMV) set by the United States. However, excess production led to Grey market sales of Japanese devices at lower prices, which in turn left an unbalanced price structure throughout the world. Companies in the United States were buying DRAM's at substantially higher prices than were Asian companies. This hurt United States electronics industry's ability to compete and thus rekindled the ire of the United States Government. Consequently, MITI asked Japan's semiconductor producers to restrict production in early 1987. This worked well because of the markets short term inelasticity. Prices immediately began to rise. Profitability soon returned to the memory market. The effect is shown below:

DRAM Manufacturing Cost Versus Price
(Worldwide Average in $)

	256K		1M	
	1987	1988	1987	1988
Price	2.54	10.00	17.87	30.00
Total Cost	3.17	3.00	11.21	10.91
Net Profit	(0.63)	7.00	6.66	19.09

110-T2

However, recent excess profits have lead to concerns about an OPEC-like control of the semiconductor market by Japan.

Nevertheless, this strategy may not work over the long term. Already, Korean producers of DRAM's are ramping up capacity that was put in place in 1986 and 1987. They are aggressively pursuing Japanese producers in the same manner that Japan pursued top American producers. Moreover, the typical group of newcomers is beginning to emerge. Already, Scott McNealy of Sun Microsystems has called for a consortium of computer makers to fund an American DRAM company. Motorola and National Semiconductor are reportedly considering reentering the market. Meanwhile, Intel steadfastly denies that it will reenter the DRAM market. This can probably be read to mean that they are in the middle of preparations to reenter the market. Consequently, another price collapse in DRAM's may well occur in the 1990 time frame.

1.1.5 Semiconductor Manufacturing Characteristics

The decision to purchase semiconductor production equipment is highly dependent on how it is to be used in a semiconductor manufacturing plant. Process flow will determine how many units will be needed. Device technology will determine the equipment performance needed. The type of

manufacturing will determine requirements for flexibility, features and configuration. The equipment chosen must closely fit the manufacturing strategy of a semiconductor company, if it is to be successful. Consequently, an understanding of manufacturing and how it affects semiconductor equipment is essential.

This section starts off with a basic explanation of the manufacturing pipeline and a description of the equipment used in a semiconductor manufacturing plant. Section 1.1.6 describes how semiconductor manufacturing has evolved from early 'R&D lab-like' manufacturing plants of the sixties to today's ultra-clean, highly automated and computerized facilities. It concludes with an in-depth assessment of likely future directions in semiconductor manufacturing. Section 1.1.7 covers basic and advanced IC processing technology. It provides a step-by-step explanation of both MOS and bipolar processes. Section 1.1.8 describes how technical driving forces shape future trends in manufacturing. It details which manufacturing parameters play an important role in determining equipment demand. It also shows how to translate technology trends in manufacturing into equipment demand.

Semiconductor Manufacturing Basics

A semiconductor manufacturing plant differs remarkably from other materials processing plants. In other types of processing plants, the material being processed usually moves through the plant in a fairly simple and straightforward in-line manner. For example, in a liquid material processing plant, the material will flow through various pipes and vats until it arrives at some final bottling point. While the flow is straightforward, a two dimensional flow chart which depicts that process will usually be quite complicated. It sometimes shows three, or even four, levels of overlapping pipes and material mixing chambers.

In contrast, the semiconductor manufacturing plant can be depicted by a very simple processing flow chart. However, material moving through the plant will follow a complex path. Often it even criss-crosses back and forth through the simplest plants. It can look like a seamless web of unending movements in a modern day flexible fab that manufactures multiple product types using multiple processes.

Consequently, this in-line characterization of a semiconductor flow-chart can be very deceptive. The complexity and reality of material flow, in contrast to an abstract flow-chart, is an extremely important concept to grasp if one is to understand the many ramifications of emerging equipment features.

Semiconductor Plant	Other Materials Plants
• Simple Material Flow Chart	• Complex Material Flow Chart
• Complex Material Movement	• Simple Material Movement

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The complete semiconductor manufacturing plant can be flow-charted in its simplest form merely by using four interconnected boxes (See Figure 1.1.5-1). A brief review will help clarify these four boxes.

Raw silicon is transformed into finished wafer slices in the wafer making stage. The end product of the wafer making stage is a polished blank wafer containing no circuitry. It is ready to start on its processing journey towards becoming a completed wafer. The industry describes this starting point in processing by the term 'wafer starts'. The wafer is then processed via numerous repetitive microlithographic, deposition, diffusion, and etching steps until it finally arrives as a finished wafer at component assembly. Here it will be diced, packaged, tested, and symbolized prior to shipment. These processes encompass three of the

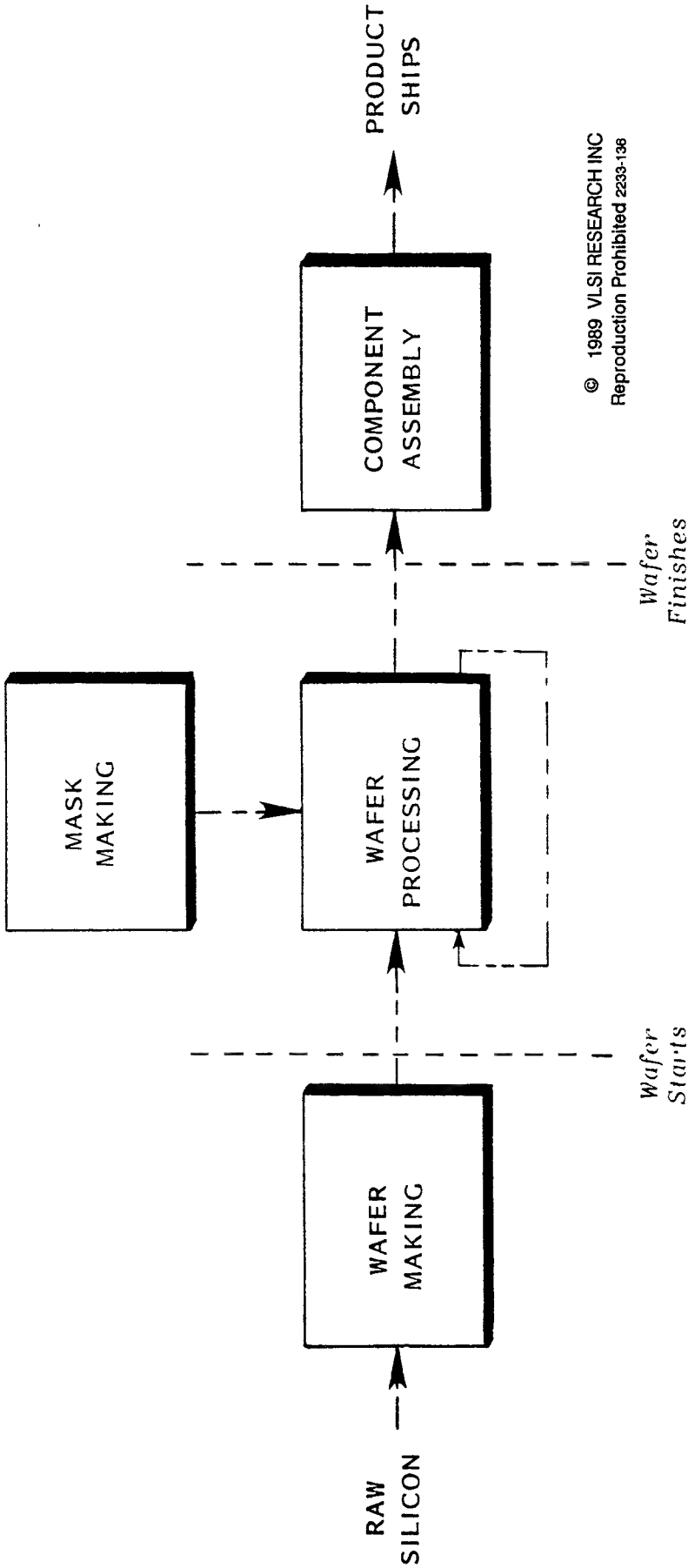


Figure 1.1.5-1

OVERALL SEMICONDUCTOR FABRICATION LINE

major steps in the flow of semiconductor material. But a fourth is needed as well—that is the mask-making activity needed to fabricate the lithographic masks which as used in defining the circuit itself.

Most modern semiconductor plants are no more complicated than this in their process flow configuration. And when these boxes are expanded further, as will be done momentarily, they merely reveal a set of some twenty-seven separate activities that follow each other step-by-step.

In actuality, most VLSI semiconductor plants are even simpler than has been depicted here. For the youngest companies, who are often the most technologically advanced do not perform wafer making. Instead, they purchase the polished wafer blanks from a separate wafer manufacturing company. These are supplied by companies such as SEH, Monsanto, or Wacker. Virtually every American company, begun after 1967, purchases the wafers it uses. This includes all of the major American integrated circuit firms such as National Semiconductor, Intel, LSI Logic, and AMD. Most Japanese companies also purchase silicon from outside vendors. Older companies such as Motorola, Fairchild, Texas Instruments and IBM still manufacture many of their own wafers. But even they have looked more and more to the purchase of wafers outside. Consequently, true VLSI semiconductor manufacturing really begins with wafer starts. This is one of the reasons why the concept of wafer starts is of such elementary importance.

A similar, but somewhat different situation prevails at mask making. A group of very sophisticated merchant mask making houses appeared after about 1965. Major ones include Master Images and Ultratech on the west coast. Qualitron and Tau Laboratories are on the east coast. Dai Nippon Screen and Toppan are in Japan. Most semiconductor firms use merchant mask makers and therefore do not manufacture their own masks. The primary reason for this has been the better quality and faster turnaround time of merchant mask makers in comparison to captive mask makers. American mask houses can typically turnaround masks in two days. Some have even achieved 24 hour turnaround times.

When these process building blocks are exploded into their constituent elements, the resulting flow chart, applicable to a VLSI factory, appears as shown in Figure 1.1.5-2. The remarkable elegance and simplicity of in-line flow is still clearly evident.

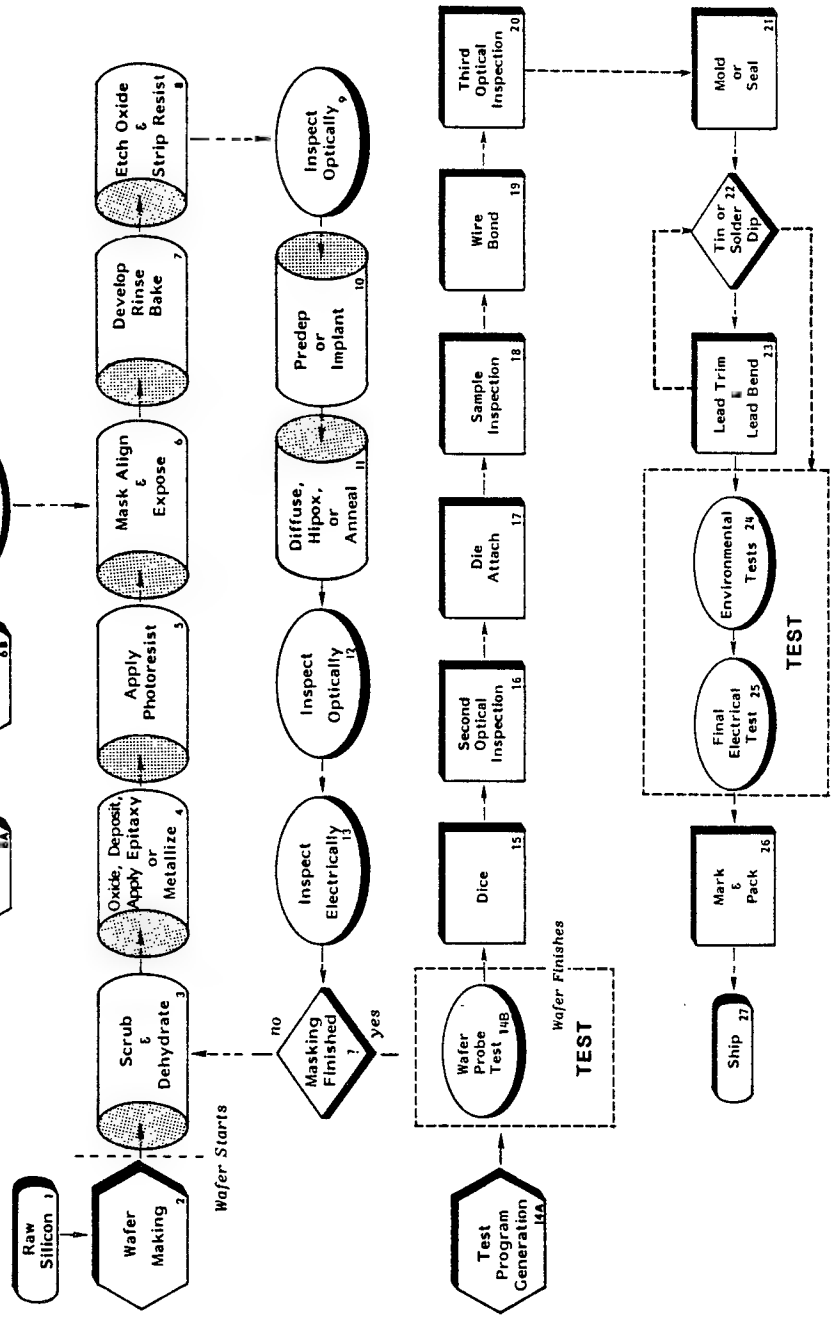
EQUIPMENT LOCATION & USAGE BY AREA

It was previously mentioned that material movement within the fab area is complex. This is because many of the steps in the process are repeated, usually several times. For example, there are more deposition steps than there are implant steps. Often, the material may not simply bypass one section. Instead, it may cross back and forth across the entire flow chart.

Similar functions are generally kept together in one area. For example, etching stations are clustered together. Likewise, a single testing area is maintained for both wafer probe tests and for final electrical tests. Inspection instruments are clustered together as well. There are at least two reasons for organizing a plant by functions rather than by its in-line operation. One is the reduction in facility support costs that can be achieved. The other is reduced operator training and greater productivity.

TABLE 1.1.5-2

TYPICAL SEMICONDUCTOR FABRICATION LINE



This is easier to envision by segmenting a semiconductor plant into its functional areas rather than by material flow. Functional areas will experience wafer processing in the amounts shown below.

Equipment is expensive, and the skills needed along the manufacturing line are simultaneously drastically different and hard to come by. But the material is small in size and can be easily transported. So it is generally more economical to transport the material back and forth between clusters of similar equipment than it is to purchase additional equipment and hire more trained operators.

Figure 1.1.5-3 shows the typical segmentation of a wafer process area. Overall, wafers move in a circular flow pattern around this process area. But individual lots will criss-cross back and forth according to the number of times they are to be processed in each functional area. The following paragraphs describe the activities of each of these functional areas and clarify this non-linear material flow.

MASK ALIGNMENT

Equipment within the alignment room, or the 'yellow room' as it is sometimes called, consists chiefly of automatic photoresist processing and alignment equipment. Etch equipment may also be in the yellow room next to mask alignment equipment or in another area. These were shown in Figure 1.1.5-2 as pipelines 3, 5, 6, 7, and 8.

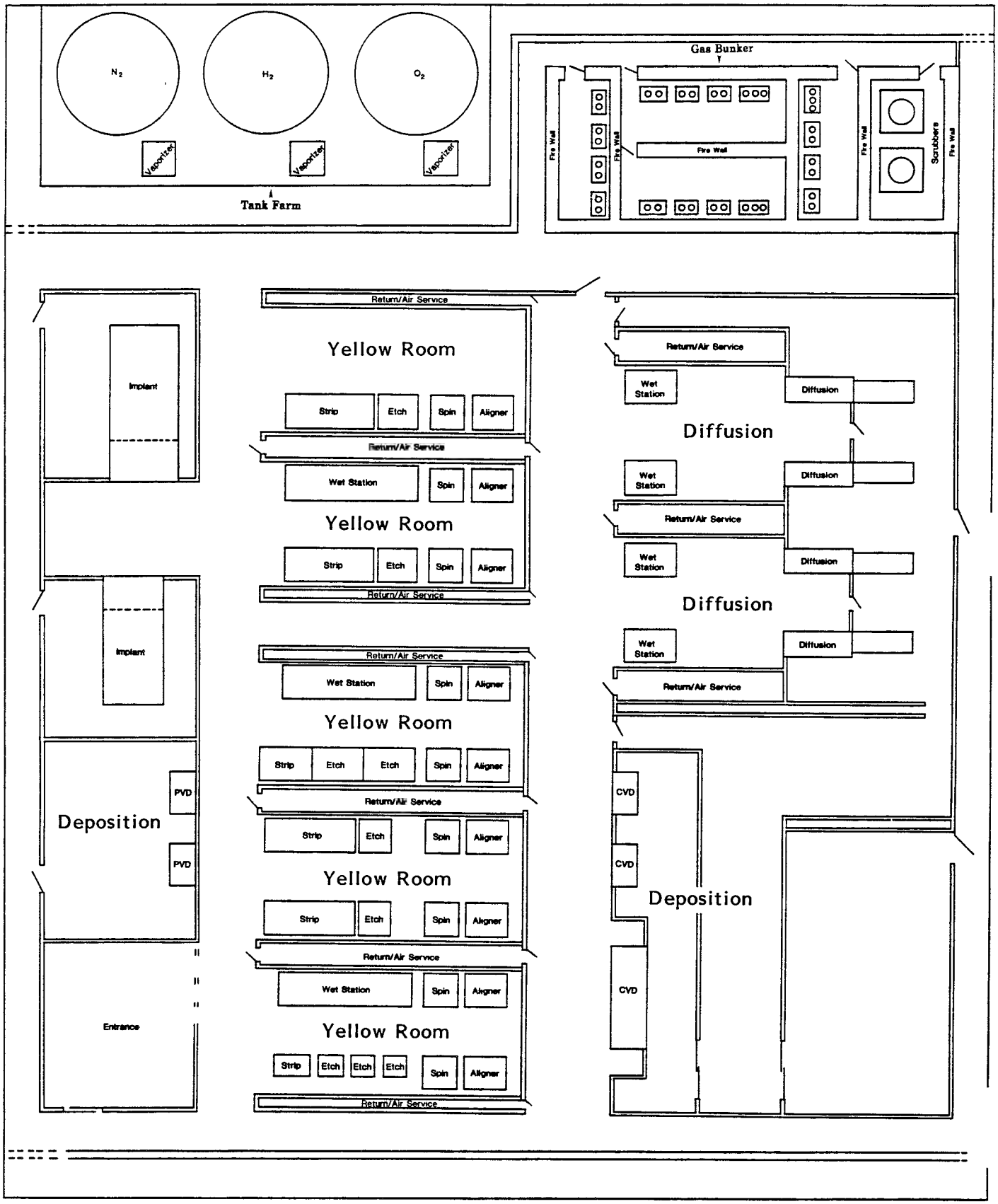
Photoresist processing equipment is often called 'track' or 'spin gear' by suppliers. Dai Nippon Screen, MTI and Silicon Valley Group are typical manufacturers. It includes all equipment which applies a photoresist to wafers and develops the exposed image. This generally includes photoresist spin-coaters, bake ovens, and spray developers. These are usually paired together. This equipment also consists of one or more tracks which move the wafer out of its cassette at an initial loading platform and then through each of these operations. Finally, it replaces the wafer in a cassette.

Manufacturing Area	*Manufacturing Function*	*Typical Number of Passess*	
		Bipolar	NMOS/CMOS
Wafer Process	Deposition	5 - 7	8 - 11
	Alignment	8 - 10	11 - 15
	Diffusion	4 - 6	7 - 10
	Etching	8 - 10	11 - 15
	Cleaning	22 - 24	29 - 39
	Inspection Stations	18 - 23	23 - 31
	Implant	2 - 6	7 - 12
Component Assembly and Test	Electrical Test	2 - 3	2 - 3
	Die & Wire Bond	1	1
	Mold or Seal	1	1
	Environmental Test	1	1

110-T4

Figure 1.1.5-3

Typical Fabline of Today



The more important operations performed are:

- Coat: Applying and spreading resists on wafers with a spinner.
- Bake: Heating after scrubbing (dehydration), after resist coating (softbake), after developing (hardbake)
- Develop: Developing circuit images that are projected onto photoresist surfaces by an aligner. Typically, the wafer is spun while developer is sprayed on it.

There are five kinds of alignment equipment in use today. Two others are being developed as well. The five existing types of aligners are contact, proximity, 1:1 projection, electron-beam direct exposure systems, and direct stepping aligners. The two types being developed are ion beam exposure systems, and X-ray exposure systems.

The following classes of alignment systems are the most widely used:

- Contact or proximity alignment: Shadow printing with light—no reduction or magnification.
- Scanning projection alignment: A full wafer photomask is subjected to a sweeping ('scan') of the light source. Mask images are projected through a mask onto a reflective lens to the wafer.
- Stepping projection alignment: An illuminated reticle is used to expose part of the wafer through a lens. The aligner then 'steps' in turn to different parts until the entire wafer is exposed to the projected pattern. Steppers use reduction ratios of 10:1, 5:1, and 1:1.
- E-beam direct exposure: An electron beam is used to directly write the patterns into the photoresist.

Contact and proximity aligners are predominantly used in older, more mature circuit technologies. They are seldom used in the manufacture of LSI or VLSI except when they are matched with more modern aligners. Projection aligners are the main workhorse of LSI. They work well at linewidths as narrow as two microns. Wafer steppers are the workhorse of most modern day VLSI manufacturing. Stepping aligners can expose lines as narrow as 0.8 microns. They may possibly go as low as 0.3 microns with future improvements. E-beam direct exposure systems are used for both ASIC and VHSIC manufacture.

Etching areas in older plants are filled with chemical etch sinks for performing etching and cleaning with acids. This is called wet-etching. Newer plants have replaced these with dry etching equipment. Plasma etchers and RIE etchers are the most commonly used dry etching equipment. Ion mills are used less frequently. Nevertheless, a modern plant still needs to have several wet stations for some etch steps. Moreover, cleaning operations are still dominated with wet processes.

Plasma 'ashers' or 'strippers' are commonly used today to remove photoresists.

DEPOSITION

Five types of capital equipment are used in the deposition area of a wafer fab. One of these is the ever-present wet cleaning equipment used to clean wafers and spin-on dopant coaters. The other four are CVD, sputtering (PVD), epitaxy and ion implantation equipment. CVD and PVD are used to deposit thin films on wafers. Epitaxy equipment is used to grow an epitaxial layer of silicon on the wafer. Ion implantation equipment is used to dope the wafer so as to alter its conductivity.

There can be as many as eleven deposition layers in an advanced CMOS circuit. Each

deposition can be classified as a conductor or a dielectric. Conductors are typically 'sandwiched' between dielectrics to form the connective wiring of an integrated circuit. Moreover, each layer can be composed of multiple depositions of films with similar electrical properties but important chemical differences. For example, a dielectric layer might be composed of a diffused thermal oxide, an LTO CVD oxide, with a nitride coating; a conductor might be composed of a titanium adhesion layer, a CVD tungsten plug in the 'contact window', a sputtered sandwich of titanium-tungsten and aluminum-copper-silicon layers.

CVD and PVD are used because of various advantages and disadvantages that are attributable to both. CVD is the most cost effective way of depositing conformal thin films. Consequently, it is used for most film layers. Its major limitation is that some films have no known chemical vapor processes, such as aluminum-copper-silicon or titanium. In these cases a sputtering system must be used. In the future, multichamber systems will be needed which offer CVD; sputtering, RTP and etch capability in the same system. The Varian M2000 is the first example of equipment that offers all four processes in a single system.

In contrast to deposition equipment, use of ion implantation is quite varied in the industry. Some advanced CMOS circuits may use as many as ten implants. While many older circuits have yet to use ion implantation. Ion implanters are typically used for about four to six applications per MOS wafer. Two are pre-deposition applications for doping the surface of the wafer. Two to four are light implants for controlling surface charge density.

There is only one epitaxial layer on a wafer. Historically, its use has been limited to bipolar devices. However, recently epitaxy has come into general use for advanced CMOS circuits.

DIFFUSION

The diffusion area consists primarily of diffusion furnaces, HiPox equipment, and rapid thermal processing (RTP) equipment. All three are used for growing thermal oxides into silicon. Diffusion furnaces are also used for many heat treatment steps such as drive-in, alloying, and reflow. They can also be configured as LPCVD furnace tubes. RTP equipment can also be used for these three steps in addition to some CVD film depositions. The lower thermal budget of RTP is its main advantage over diffusion. However, diffusion is more cost effective. Consequently, both types of equipment can be found in an advanced wafer fab.

INSPECTION STATIONS

The types of equipment that can be found in the typical inspection area of a wafer fab are quite diverse. Moreover, inspection equipment can also be found throughout the other areas of fab. Inspection has benefited strongly from the advent of VLSI. Film quality is a critical factor in manufacturing VLSI circuitry. Consequently, highly specialized and more automated inspection equipment has become needed. Automatic inspection stations have evolved from microscopes. Automatic inspection for particulates, defects, film composition, critical dimension measuring, and wafer profiling are now commonplace.

Electrical inspection stations consist of curve tracers and process monitoring systems. Process monitors are more like automatic test systems. They are only different in the sense that the tests to be made are dominantly used for determining physical parameters, not for determining electrical parameters. In addition to these larger systems, there are also several test instruments that should be included in this grouping. These consist of four-point probes, CV plotters, film-thickness measuring,

and a few others. However, all of these machines are used sporadically, consequently the overall market is small.

TESTING AREA

When a wafer moves to the test area, it leaves wafer processing. It also leaves the clean room environment forever. The testing area is usually a large segregated area that provides no other function. Capital equipment in the test area includes automatic test equipment, wafer probing equipment, package handling equipment, automatic process monitors, and curve tracers. There is no other capital equipment used there except for a few test instruments and oscilloscopes whose purpose is to support the major test equipment.

ASSEMBLY AREA

The main assembly area usually contains dicing saws, die attach equipment, wire bonding equipment, and second and third optical inspection. Packaging, molding, lid sealing and environmental testing is usually performed in adjacent areas that are not as clean as the main assembly area.

1.1.6 Development of the Semiconductor Manufacturing Industry

It has been a remarkably short time since the invention of the transistor in 1947, and shorter still since the invention of the integrated circuit in 1959. By 1952–just five years after invention of the transistor–Western Electric had issued twenty-six licenses within the United States and nine to foreign licensees. Normally, many more years are needed before an invention can be introduced into the commercial marketplace. For example, the interval between invention of penicillin and it's commercial introduction was 16 years. In contrast, that of nylon was 11 years. Polyester fiber took 12 years, while radar took 13 and television 22.

This primarily-American success story is a fascinating one which most everyone knows by now.† At Bell Laboratories, in December 1947, Bardeen and Brattain had demonstrated the amplifying characteristics of a germanium-based, point-contact transistor. As part of a semiconductor research group under the leadership of William Shockley, Bardeen and Brattain received a patent for their invention and, on June 30, 1948, held the first public exhibition of the device in New York.

Publicity of the transistor's invention gained widespread attention. But it was AT&T's unusually benevolent attitude that ensured the early success of the transistor. AT&T had recognized that it held the keys to an industrial revolution. So the decision was made to license the manufacturing rights for the nominally small fee of just $25,000 to all interested parties. AT&T even published a series of well-known manufacturing textbooks to help ensure transfer of the technology. No series of textbooks since then have disclosed such depth of manufacturing technology as did these books.

Early licensees of the transistors included many of today's giants. Names such as Texas Instruments, IBM, RCA, General Electric and Motorola were there. It also included some who are hardly known today as semiconductor suppliers: Westinghouse, Sylvania and Philco. Some companies, such as General Electric, became early failures who exited the market and then re-entered many years later.

As these licensees geared up for the manufacture of semiconductors, a creative spurt in manufacturing was unleashed which has yet to run its course. Moreover, this semiconductor manufacturing acumen has be-

† See, for example, "The Solid State Era", Electronics, April 17, 1980, pp. 215.

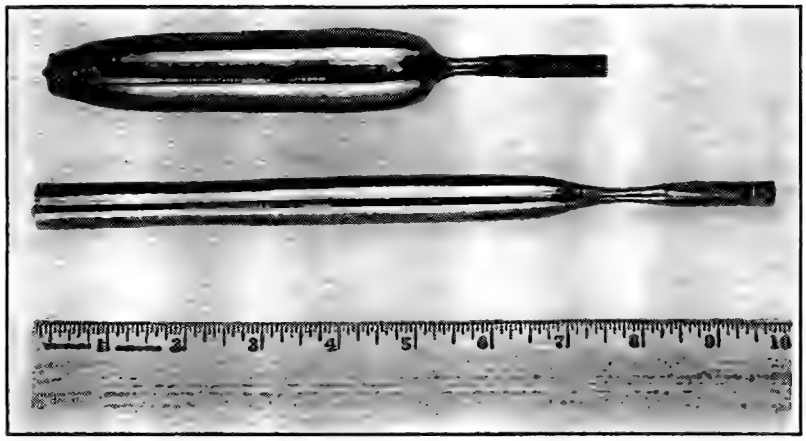
come general enough to have spilled over into other manufacturing arenas such as hard-disk drives, flat-panel displays, and even superconductors. This, in turn, is creating still more manufacturing revolutions.

1.1.6.1 Comparison of Early and Modern Manufacturing Equipment

To understand these forces, it is helpful to turn back the clock and examine some of the methods used earlier and then to contrast them with those used now. A good starting place is to examine the growth of ingots.

The very first commercial silicon ingots were about 3/4 inch in diameter, as seen in Figure 1.1.6.1-1.

Contrast these with today's more commonplace three, four and five inch ingots—Figure 1.1.6.1-2. One might think that advancements in the crystal growing furnaces primarily contributed to this growth in ingot size. In truth, however, it was the processing equipment which proved to be the more significant limitation and which required the more significant advancements.



Ref: Phillips, Transistor Engineering, 1962, p.7

Figure 1.1.6.1-1 2233-139

Early Ingots of Germanium and Silicon

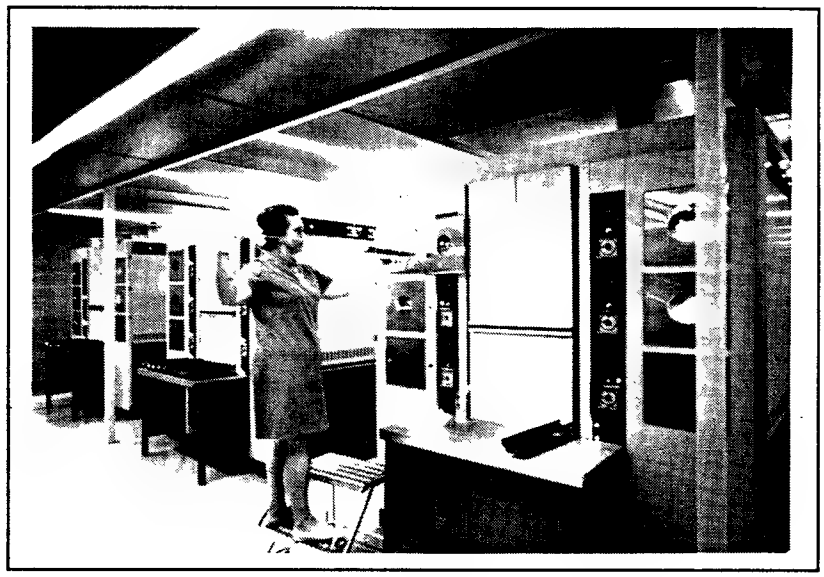
Figure 1.1.6.1-2 Courtesy: Komatsu 2233-140

Modern Ingots

At first the equipment posed little difficulty. Introduction of larger diameter wafers made from two and three inch diameter ingots was easily enough adapted. Four inch wafers were introduced in 1974.

These created somewhat more difficulty and caused much concern. Wafer flatness was hard to hold across four inches. Moreover, lens limits were beginning to be reached by such large areas. Still, four inch wafers caught on rapidly.

Five inch wafers were introduced in 1979. These proved quite difficult. Diffusion furnace tubes now had such large openings that temperature profiles could not be maintained. Plastic distortion raised concerns about the so-called 'continental drift' –i.e.–localized shifts of components within the wafer. For the first time, taperof the wafer created enough problems that Z-axis control had to be added to probers and aligners.



Courtesy: Al Stein, VTI

Figure 1.1.6.1-3
2233-141

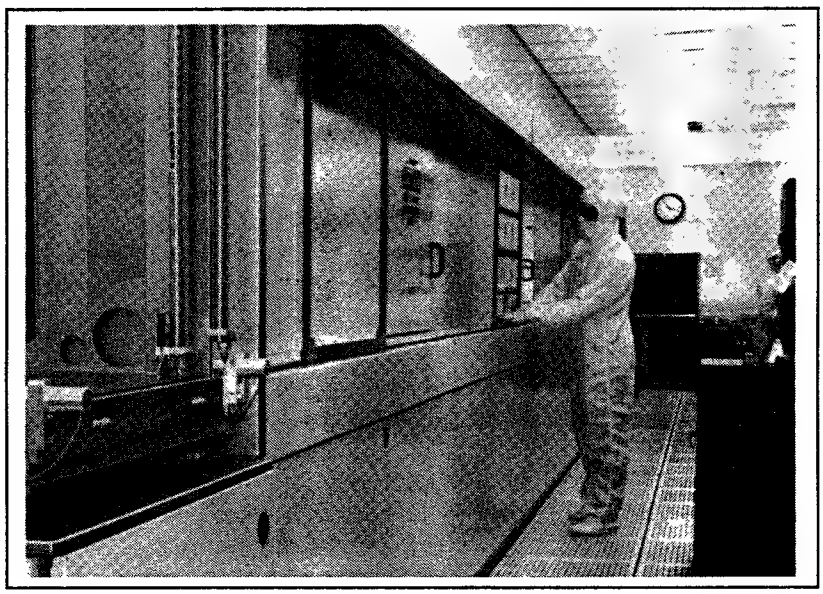
Early-Day Diffusion Operation

Particulate control methods evolved along with the wafers. Clean room garments were seldom required early on. Street clothes were still being permitted in process areas, as late as the mid-seventies, as can be seen by the early-day diffusion operator in Figure 1.1.6.1-3. Clean room classes were of the order of class 5000 to 10,000, but no one was monitoring it so the actual counts are known more by reference to today's standards of Class 1 to Class 10, as shown in Figure 1.1.6.1-4.

Understanding of cleanliness requirements and their adaptations was a slow and arduous task. One early example was amusing but also enlightening: It had been noted that periodic losses of the processing menu had been occurring in one line in Palo Alto. These losses were eventually traced to excess phosphorus. The phosphorus was subsequently discovered to be coming from lawn fertilizer outside the building. It occurred each time the gardener fertilized–likely through an open window. Today we would find it incomprehensible that such gross impurities would drift into a clean room.

Equipment setup and repair was also found to contribute substantially to contamination. Note from Figure 1.1.6.1-4 how laminar air flow is now maintained and that equipment walls are totally vertical.Contrast this with the very open areas around the early evaporation equipment shown in Figure 1.1.6.1-5. In turn, compare this evaporation equipment, with its modern-day counterpart, as shown in Figure 1.1.6.1-6.

Much of the development in equipment centered around improvements such as this.

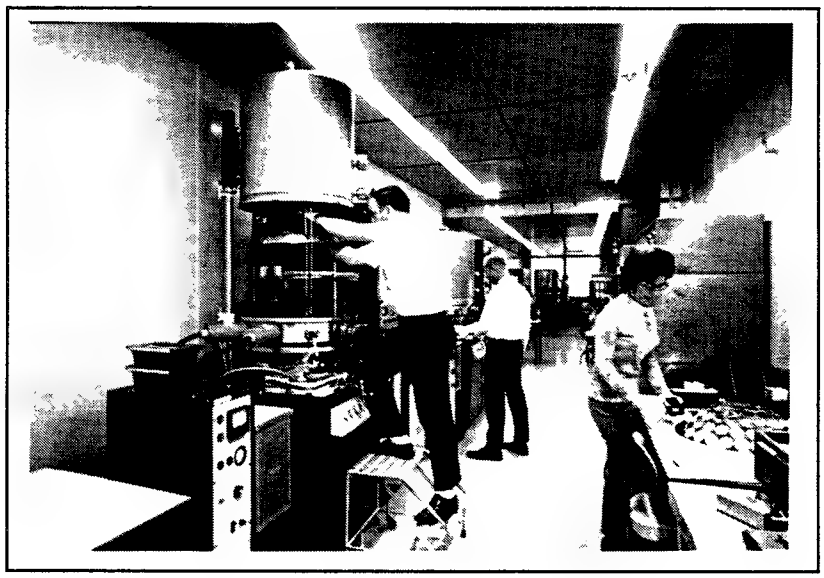


Ref: Microcontamination, Aug. 1987, P.29

2233-142

Figure 1.1.6.1-4

Modern Clean Room Activity



Courtesy: Al Stein, VTI

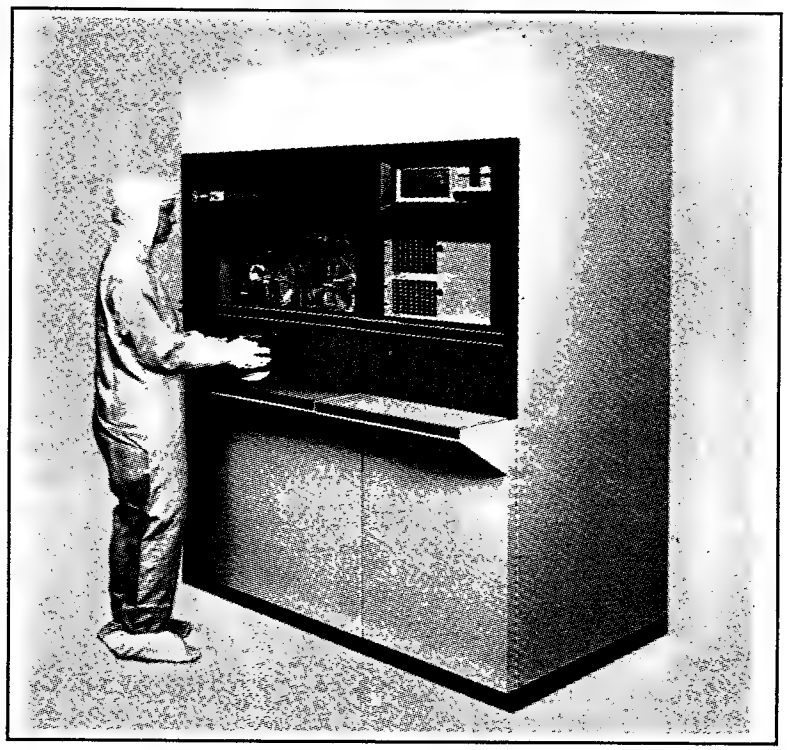
2233-143

Figure 1.1.6.1-5

Early-Day Evaporation System

1.1.6.2 Emerence of Modern Manufacturing Equipment

Modern semiconductor manufacturing equipment began to emerge in the early seventies. This emergence was found to be more evolutionary than it was revolutionary. It was driven by issues concerning yield, automation and cost, just as today. In-line automation concepts were also being attempted as early as 1961 or 1962. Most of these attempts centered around continuous vacuum equip-ment rather than interconnected equipment. The results were largely unsuccessful and equipment remained as discrete standalone units.



Courtesy: Varian
2233-144

Figure 1.1.6.1-6
Modern Sputtering System

The first truly-successful modern equipment was resist processing equipment. It was supplied by GCA at the time, and by Kasper Instruments (now Eaton) shortly thereafter. Figure 1.1.6.2-1 depicts a manual resist spin-on system of the late sixties.

In it, the two-inch wafers are manually placed on the spinner with tweezers. Resist is sprayed on from the plastic hand-held dispenser. Contrast this with a modern resist processing system from Silicon Valley Group, as depicted in Figure 1.1.6.2-2. In this system, wafers are automatically taken from and then returned to wafer cassettes via elevator indexers. Spin, bake and develop are automatic. A small computer operates as a controller to completely operate the system.

The emergence of manufacturing equipment from all areas of the fabline largely follows a development path similar to that of resist processing equipment. Several quite-distinct evolutionary phases occur. They are:

Stage 1: Equipment Cluster Integration
Stage 2: Dedicated Equipment Applications
Stage 3: General Purpose Equipment Applications
Stage 4: Manufacturing Differentiation
Stage 5: System Cluster Integration

Stage 1 invariably consists of simply tying together a set of adjacent, but quite separate operations and then integrating them—virtually unchanged—into a single system. Automatic test equipment and resist processing equipment underwent Stage 1 in its evolution more than twenty years ago. Linewidth measuring equipment has just

emerged from this stage. Liquid and gas monitoring systems are just entering it.

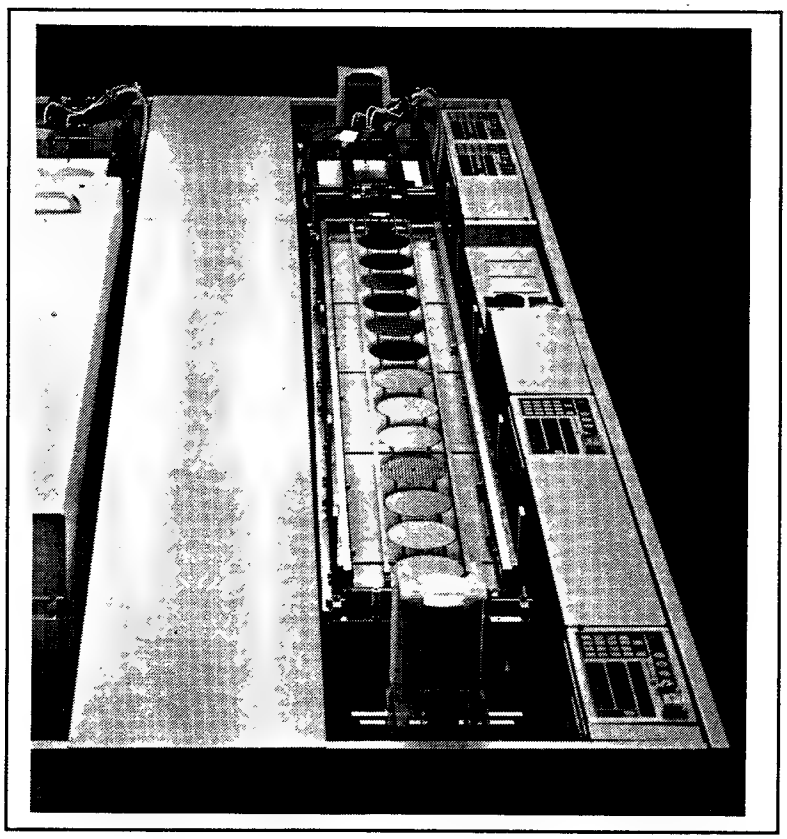
Stage 2 represents a high growth non-equilibrium period. The systems in Stage 2 are redesigned to accomplish some specific task at hand. They become highly specialized and very dedicated tools. No -longer-needed obsolete appendages that were mere vestiges of the pre-integrated applications are stripped away while new, more useful, functions are added. CIM systems (Computer Integrated Manufacturing) are at this stage today in semiconductor manufacturing.

Courtesy: Al Stein, VTI
2233-145

Figure 1.1.6.2-1
Early-Day Resist Dispensing

Stage 3 comes into existence when the product reaches initial maturity. At this time, the market comes into equilibrium and grows at a rather constant rate. Issues tend to center around execution—how good and how much. Changes of features settle down to become well orchestrated feature improvements. Stepping aligners and ion implanters are at this stage today.

Stage 4 represents old age, in one manner of speaking, while it represents a rebirth in another. When equipment reaches Stage 4, it is often characterized as being 'stripped down for manufacturing'. Usually those features not needed by a manufacturer have been totally stripped away. The machine now excels at high volume ma-



Courtesy: SVG
2233-146

Figure 1.1.6.2-2
Modern Resist Processing System

nufacturing. Automatic test equipment and diffusion furnaces are now at this stage.

Stage 5 represents a metamorphosis. Equipment emerges from a larva-like existence of Stage 4 into a new butterfly-like Stage 5 existence. At Stage 5, entire systems are now integrated into single superclusters.

The life cycle then begins anew. Multi-processing CVD systems, including etch and sputtering, are at this stage today. So, too, is the laser pantograph—the first rudimentary chip dispensing machine.

In this panorama of evolution, one finds a continuum of change in equipment. Almost invariably, semiconductor linewidth comes to play a central role as the figure of merit. Many people bandy-about the concept of one micron lines-and-spaces as being a most significant measure of advancement. Consequently, the time-rate-of-change of achievable linewidth has often been used as a gauge of advance ment. But this is an elusive gauge, for few such forecasts of linewidth improvement over time have ever come to pass. Figure 1.1.6.2-3 reproduces what was probably the very earliest attempt to predict semiconductor technology via linewidth improvements.

It was published by H. Wolf and K. Greenough back in 1967. At the time, Wolf and Greenough projected that an order-of-magnitude decrease in linewidth would occur every seven years. They even predicted that production linewidths would reach 0.6 microns by 1970. At the time this was about three years into the future. Figure 1.1.6.2-4 represents an up-to-date version. This chart predicts that production linewidths will reach 0.6 microns by 1990—again about three years into the future! Although twenty-one years have elapsed, linewidth projections have hardly changed between these two charts. Consequently it can be concluded that linewidth has not proven to be a good gauge of technological progress of modern semiconductor equipment.

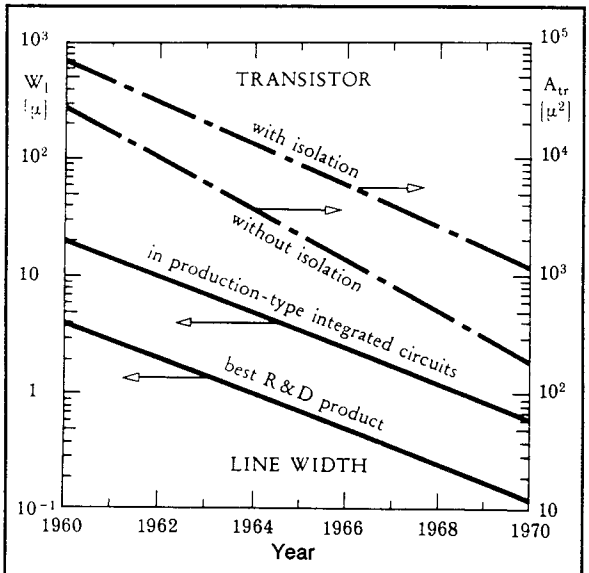


Figure 1.1.6.2-3

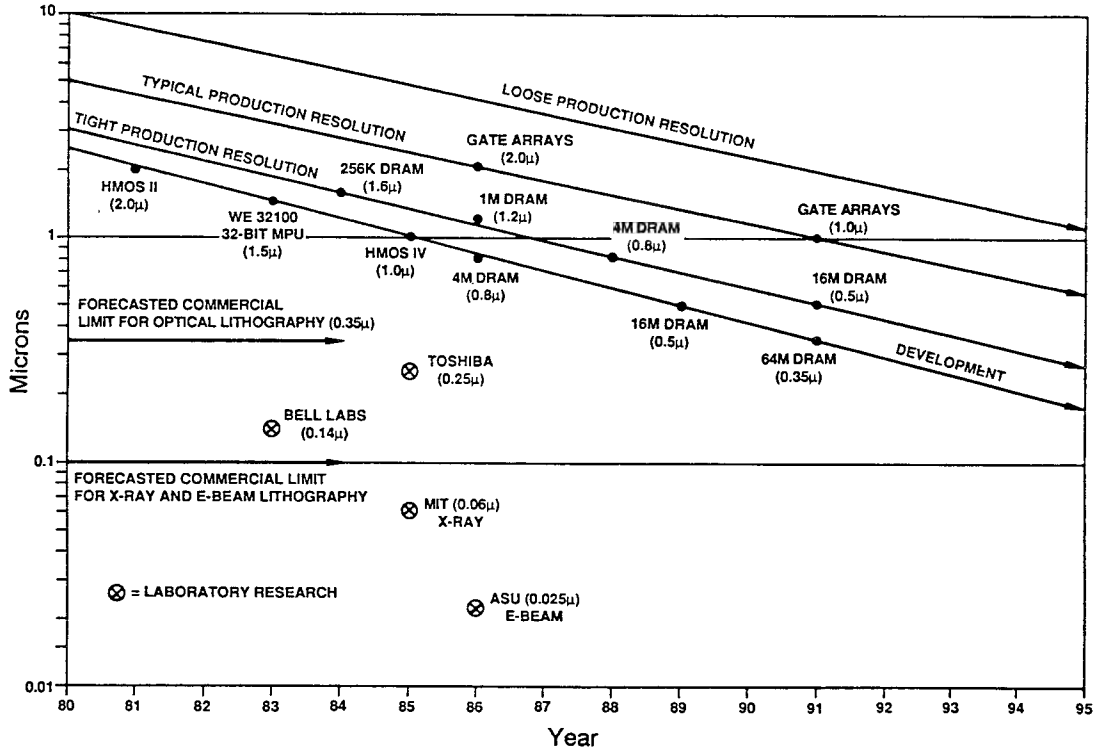
Smallest line width (W_l) and transistor area (A_{tr}) for various years, as projected in 1967.

Ref: Wolf & Greenough, Microelectronics and Reliability, 1967, Vol.6, P.292 2233-147

1.1.6.3 Beginning of Integrated Factories

Many approaches to fully integrated factories had been speculated about, and even tried by the early sixties. But most failed to develop because of lack of flexibility in manufacturing. Almost every attempt at integrating a factory was found to favor the supplier while it disfavored the customer. This was because of one fundamental limitation: Most automated lines, when producing at optimized costs, need to be very finely tuned to produce a fixed quantity of shipments per accounting period. But most customers have found that their individual order rates varied widely on a month-to-month basis. These so-called 'flexible manufacturing systems' simply were not flexible enough to meet such varying customer demands. So they were torn down. This same weakness has plagued the industry in more recent times. The highly efficient DRAM factory is one case in point.

During the early eighties, it was also thought that transport systems would be used by



Source: ICE, 1988, P.5-21

2233-148

Figure 1.1.6.2-4

IC Feature Size Trends as Projected in 1988

industry. These were conceived as consisting of clean tunnels containing rows of moving cassettes or rows of moving wafers. It was also thought that lithography and ion implant would be the first areas to be integrated. Figure 1.1.6.3-1 depicts one concept of the early eighties.

Such conceptual lines were actually built. IBM built two such lines and called them QTAT lines, for Quick TurnAround Tools. Both lines were eventually dismounted after some three or four years of operation. NMB next built a line based upon robots and transfer systems moving along fixed corridors. That plant, outside Tokyo in Tateyama, is still extant.

Tunnel type units eventually failed. This occurred partly because users found them too difficult to keep clean; partly because they were customer insensitive; and partly because having once been installed, they were too difficult to modify. First IBM, and then Varian, attempted to build clean tunnels between equipment. Both attempts failed.

Still, the concept of integrated, fully automated, factories provided a compelling architecture. First, they were dubbed sand-in finished product-out factories. Next they were called islands-of-automation. Eventually they came be called 'lights out' factories. Clearly, these concepts were too distant for practicality. Next, Veeco and the Flexible Manufacturing Systems Corporation attempted solutions. Their approach was to use guided vehicles as the cassette transportation mechanism. Veeco used a guided wire approach. FMS used infrared communication. Figure 1.6.1.3-2 depicts

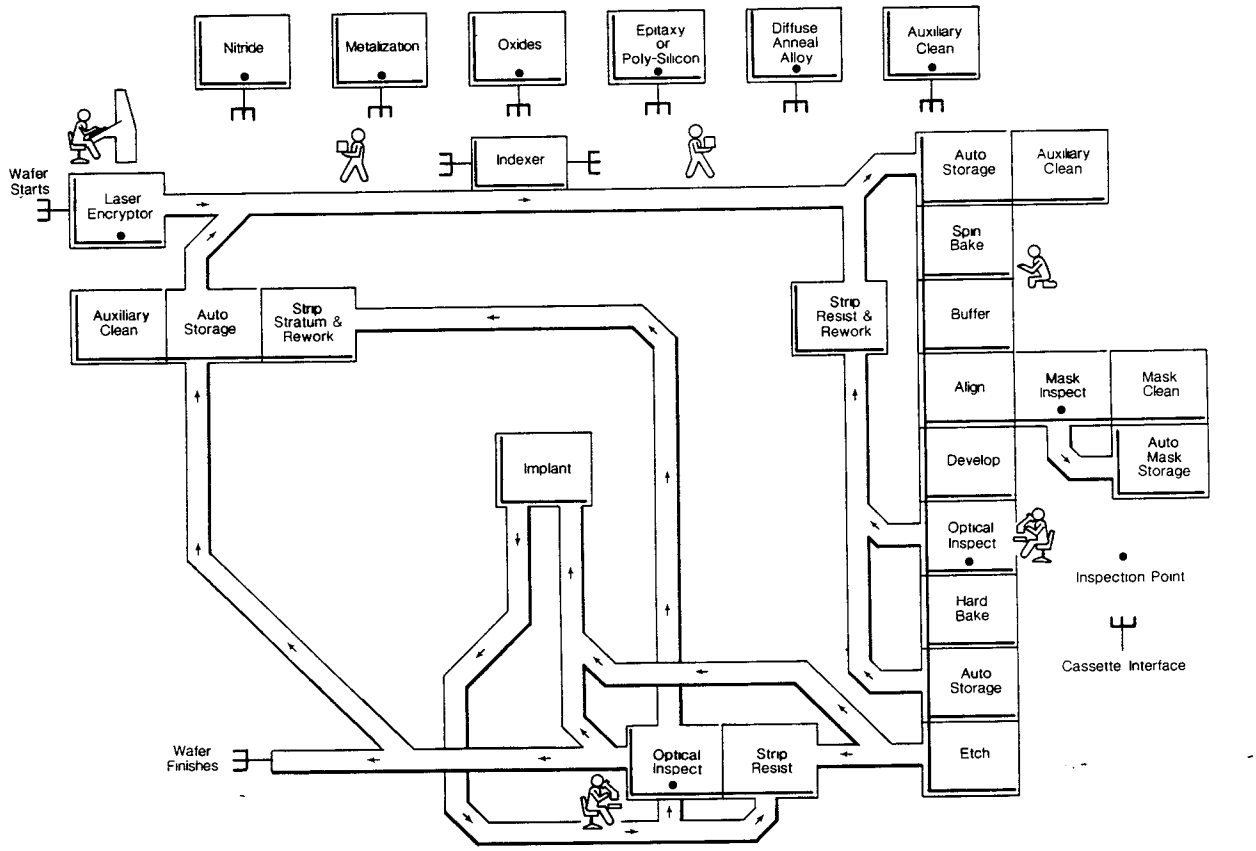


Figure 1.1.6.3-1

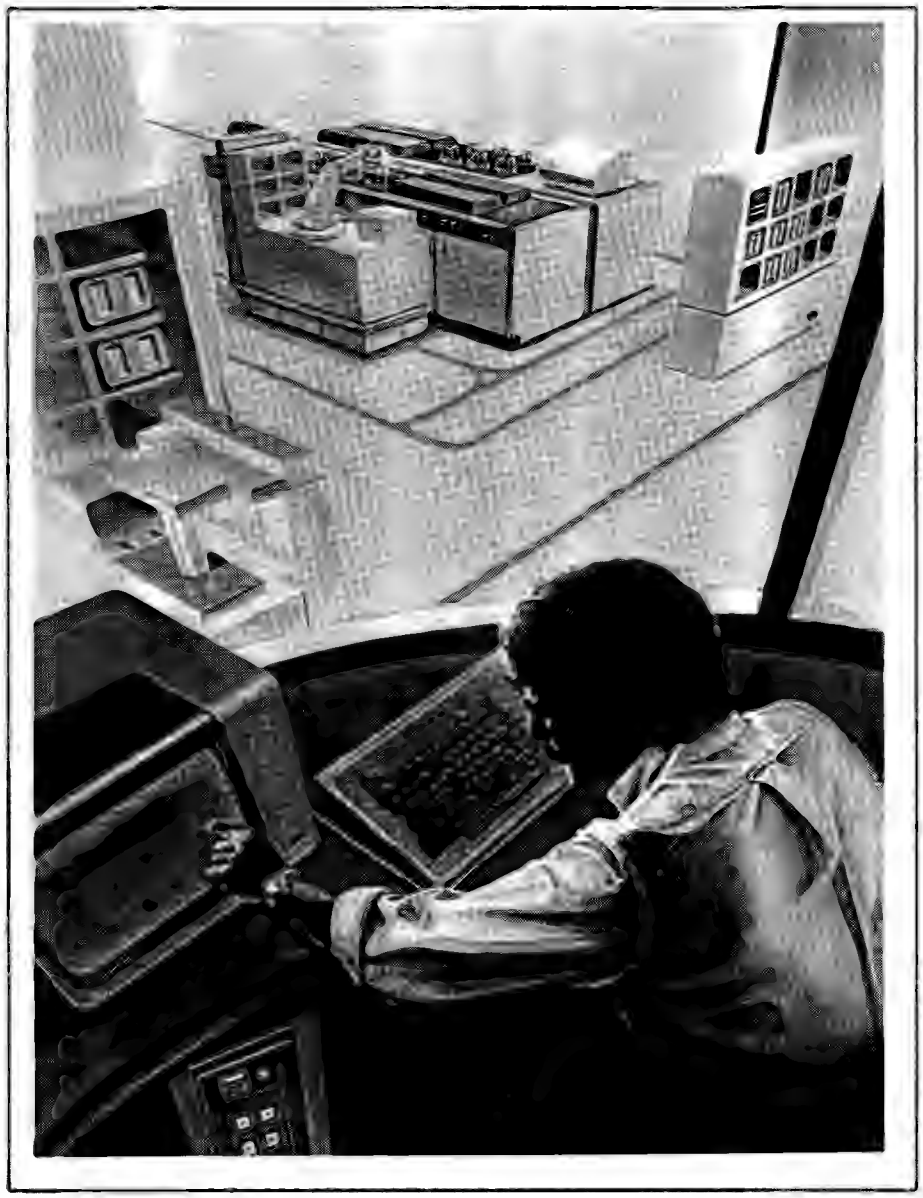
THE PROCESS LINE OF THE FUTURE AS PERCEIVED AROUND 1982

Veeco's concept of an integrated factory, as viewed from a hypothetical command post. Guided vehicles can be seen in the background, tracking along imbedded wires buried in the striped guideways appearing on the floor. Figure 1.6.1.3-3 depicts the various elements available with Veeco's integrated approach.

Such systems have proven to be more viable than were transport tunnels. Still, they have yet to catch on within the general industry.

During this time it was also found that the so-called islands-of-automation would likely succeed, but only in lithography. Resist Processing Systems had already been integrated to the degree necessary. But what was not foreseen at the time was a growing interdependence between sputtering systems, etch systems, CVD systems and cleaning systems. This interdependence was not anticipated in the early eighties. Rather, as was depicted in Figure 1.1.6.3-1, it was thought that these systems would remain separate entities. Instead, the interdependences between equipment has thrust the equipment together and resulted in "multiprocessing systems".

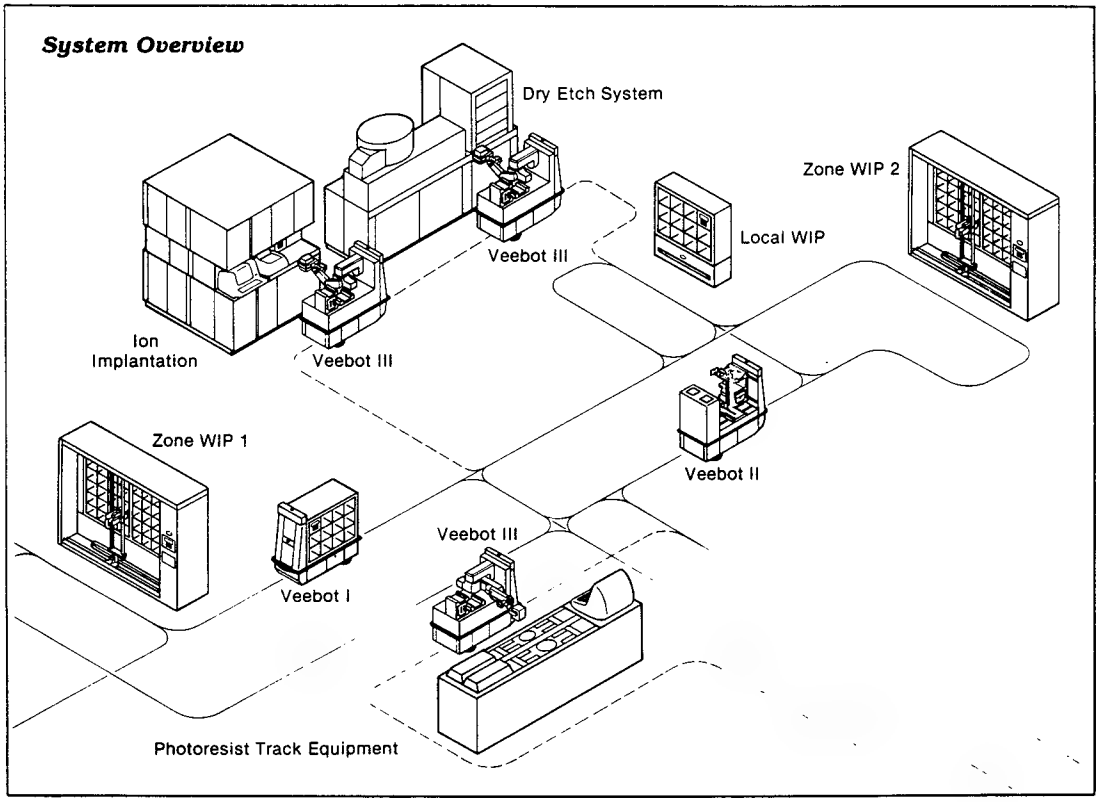
Figure 1.6.1.3-4 depicts such a typical multiprocessing system. This is the Applied Materials' Precision 5000 CVD System. It makes use of several independent chambers clustered around a cassette input/output module. Each chamber can conduct a se-



Ref: VEECO
2233-150

Figure 1.1.6.3-2

VEECO'S FLEXIBLE AUTOMATED WAFER FAB SYSTEMS



Ref: VEECO
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Figure 1.1.6.3-3

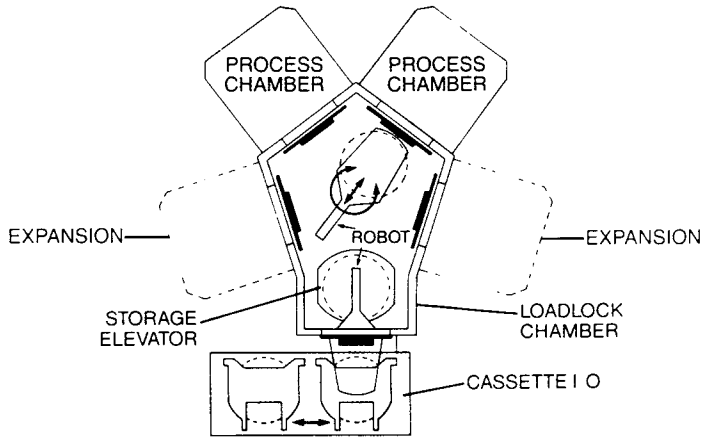
VEECO'S Flexible Automation System

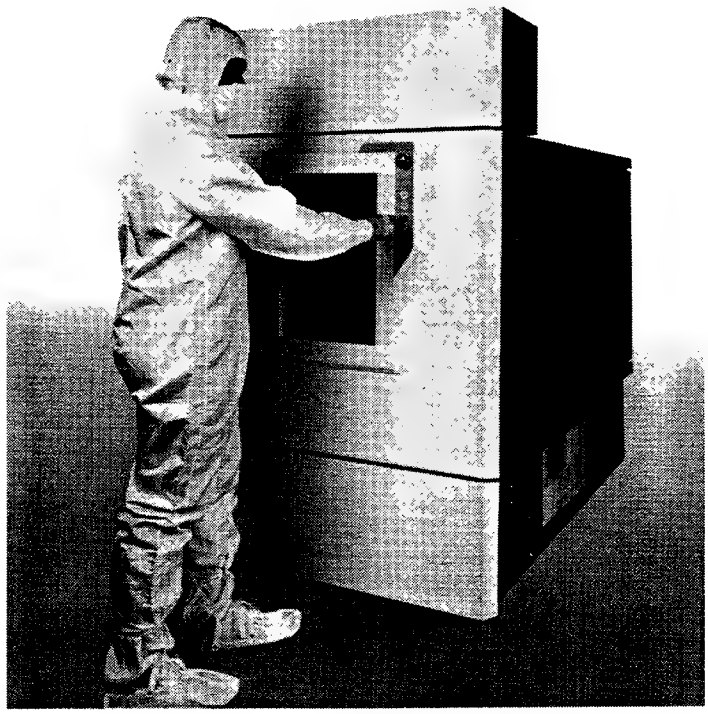
parate operation. Such systems foreshadow several evolving concepts of modern semiconductor factories.

The first of these is the clear cut indication that clean rooms are folding inside the equipment. Less and less protection of the wafer is needed outside the processing equipment. Moreover, space-suit-like protective enclosures such as Asyst's SMIF are both eliminating the need to protect the wafer in routine environments. Second, single systems are taking on the aspects of entire clusters of manufacturing as the industry enters Stage 1 of a new generation of factories (see previous section). Third, all systems are rapidly shrinking in size and are approaching the size of dispensing machines, suggesting that, in time, semiconductor manufacturing facilities may be reduced to small chip dispensing machines installed on a system manufacturers' factory floor, and becoming just another tool rather than a full factory.

1.6.1.4 Likely Future Directions

From the vantage point presented in the past few sections, it can now be more easily seen that factory evolution has centered dominantly around yield improvements, clean room improvements, and wafer size improvements. Automation has proceeded slowly but dramatically; but its greatest achievements have been mostly in terms of 'under-the-hood' advancements, leading to smarter machines rather than more integrated factories and to more integration within single machines.





Courtesy: AMT
2233-152

Figure 1.1.6.3-4

The AMT Precision 5000 CVD

TABLE 1.1.6.4-1

MANUFACTURING DEVELOPMENT

Item	*1965*	*1975*	*1985*
Cost of Fab	$1M	$9M	$100M
Automation	Manual	Semi-Autoload	Cassette to Cassette
Leading Wafer Size	1¼"	4"	5"
Production Linewidth	6-12μ	3-6μ	1.5-3μ
Production Registration	2-3μ	0.5-1μ	0.2-0.5μ
Clean Room Class	10,000?	1,000	10
Product Class	SSI	LSI	VLSI
# Components	10	1,000	1,000,000
Workers Garments	Lab Coats	Smocks	Bunny Suits
Where Located	Spread Around U.S.	Silicon Valley Clusters	W.W.
Engineering Tools	Rotary Calculator	Electronic Calculator	Workstations

This evolutionary trend is depicted on a more panoramic basis in Table 1.6.1.4-1. Fabrication facility costs have risen directly from about $1M in 1968, to some $9M by 1975, and then to $100M by 1985. This rate of increase is about one decade in cost, per decade in time. At such a rate, 1995 fabs may well cost $1B. Meanwhile wafer sizes have moved from one-and-one-quarter-inch diameters in 1965 to six inch diameters by 1985. Eight inch wafers were introduced in 1987, thus representing a doubling in wafer diameters every thirteen years. If this rate of introduction continues, sixteen inch wafers can be expected by the late nineties. While the continuation of both of these trends may be possible, it hardly seems likely. Slowing trends are already coming into evidence. Customers are realizing they simply cannot afford more expensive factories. The economics that led to larger wafers peaked at six inch sizes.

Other trends are depicted in the table also. Among these, linewidths are the most often used as a measure of future direction. But as noted in the previous section, future projections of linewidth sizes below one micron have changed little in the past twenty years. As noted in the tables however, there have been slower, more evolutionary, improvements in linewidth over this time. Several difficulties arise when using linewidth as a tool for projecting future markets. One important difficulty has to do with the fact that almost all linewidth projections assume that IC design methods will remain the same and that lithographic methods will remain planar—i.e.—two dimensional films will be used to pattern the devices. In point of fact however, substantial numbers of vertical processing techniques—i.e.—three dimensional patterning methods—are beginning to make an appearance.

A second limitation deals with a very often neglected empirical rule about the lenses that are used in lithography. That rule states that all lenses reach their limit of ability when the image pixel quantity reaches about one hundred million pixels. This limit will be reached with dynamic RAMS of about 24 megabits in size. But sixteen megabit DRAMs are already on the drawing boards. Moreover the Sematech criteria calls for one-half micron lines on 5.5 millimeter chips by 1992. Such chips would need 121 million pixels. This pixel quantity is more than five times better than the best current lenses can produce. For this to happen, therefore, dramatic improvements in lenses must be achieved. But there are little developments on the horizon which indicate the methodology will be found. Consequently, it can be expected that linewidth, as a measure of the leading edge of chip manufacturing will gradually give way to some other approach. New manufacturing methods which will mitigate the need for ever-smaller lines will likely evolve. Three dimensional patterning suggests the industry is taking a lesson from nature and folding the surfaces to obtain larger surface area, just as is done in the brain and the intestine. As this happens, the industry may not need to go below one-half micron linewidths to achieve its objectives. Our industry's conceptual models of future factories may need to be altered.

Other difficulties arise when attempting to predict both the quantities and the types of factories by merely extrapolating today's issues. For instance, the DRAM factory has been the most successfully modeled of all semiconductor factories, on an economic basis. In fact it is not untruthful to state it has been the only successfully modeled factory. Other types of factories are far less well understood. As a result, virtually all economic models use the DRAM factory as a starting point. But this type of factory has been optimized for extremely high-volume throughput, while producing just a few product types. A DRAM factory operates at about 2/3 utility when running just two-or-three product types. But when producing between five-to-seven product types, utilization drops to fifty percent of that obtained for one product type. In contrast, standard-product factories may need to simultaneously run as many as twenty product types, while an ASIC factory may need to run more than fifty.

DRAM factories are optimized for very high volume and can handle such few part types. But standard factories and ASIC factories don't run well at such high volumes while simultaneously manufacturing many different product types. Consequently, they tend to be smaller, their equipment operating schedules tend to be much less well balanced, and queing problems tend to be dynamic, hopping from one area to another as the factory adjusts to simultaneous fat/lean situations across its entire floor.

These pressures will likely lead to a split in manufacturing styles. Smaller factories that make use of more adaptive machines, more broadly skilled people, and enormously more complicated software will arise to handle both ASIC factories and small standard-product factories. Their activities will emphasize and favor short setup times and

extreme flexibility. High volume equipment for DRAM types of factories will emphasize throughput, uniformity and batch processing.

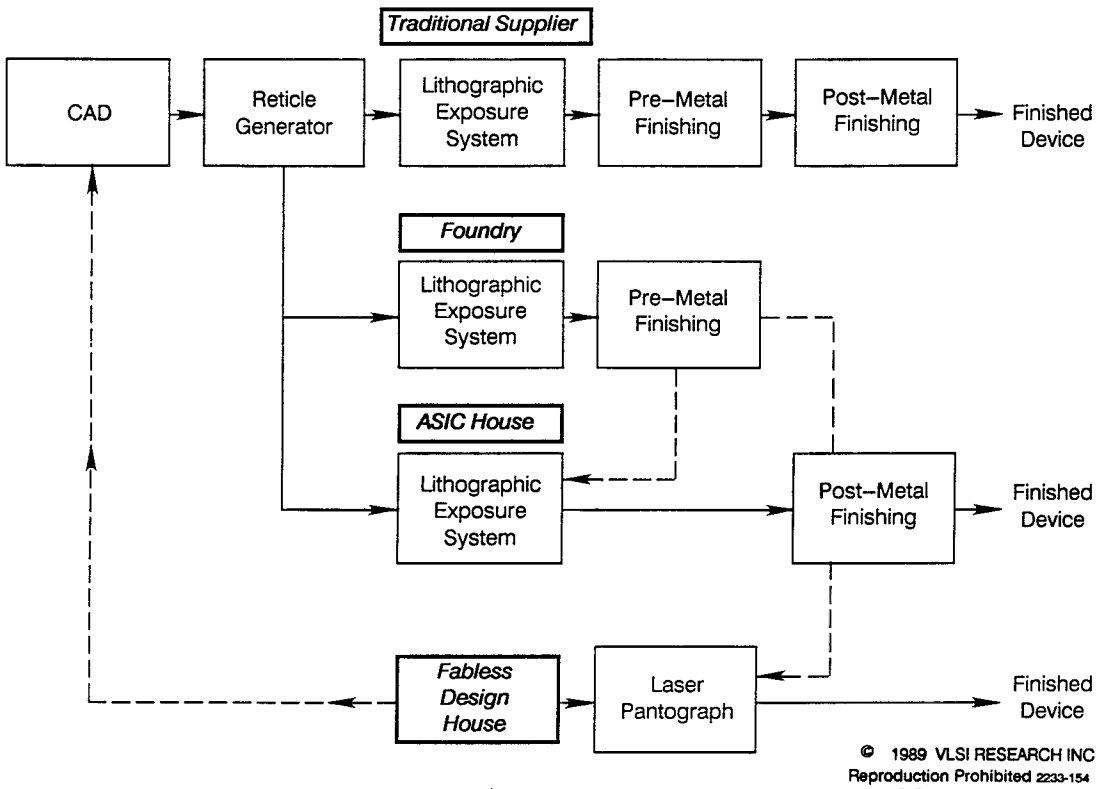
There is enough demand on the world scene for about ten to fifteen of these highly efficient DRAM factories. But political pressures to maintain national capabilities will likely keep this above twenty such factories. This, in turn, will likely lead to perpetually excessive DRAM capacity, to continuously collapsing DRAM prices and to governmental regulations. Equipment for these factories will be exceptionally efficient, very high throughput, and almost totally operator-less.

Figure 1.6.1.4-2 depicts how it is currently believed that factories are evolving. The top line in the figure represents a standard factory, including a DRAM factory. The ASIC houses and foundries are developing jointly, with foundries supplying the pre-metal finishing while ASICs provide post-metal processing and chip 'personalization'. ASIC houses are generating demand for a designer middleman. This is coming to be the fabless design house. It has design specialists, but no processing capability. These middlemen design the product, and then contract its manufacture with the ASIC house, which in turn looks to the foundry for the substrate. The laser pantograph—progenitor of true chip dispensing machines—has come about to bridge the ASIC house, and to produce chips directly.

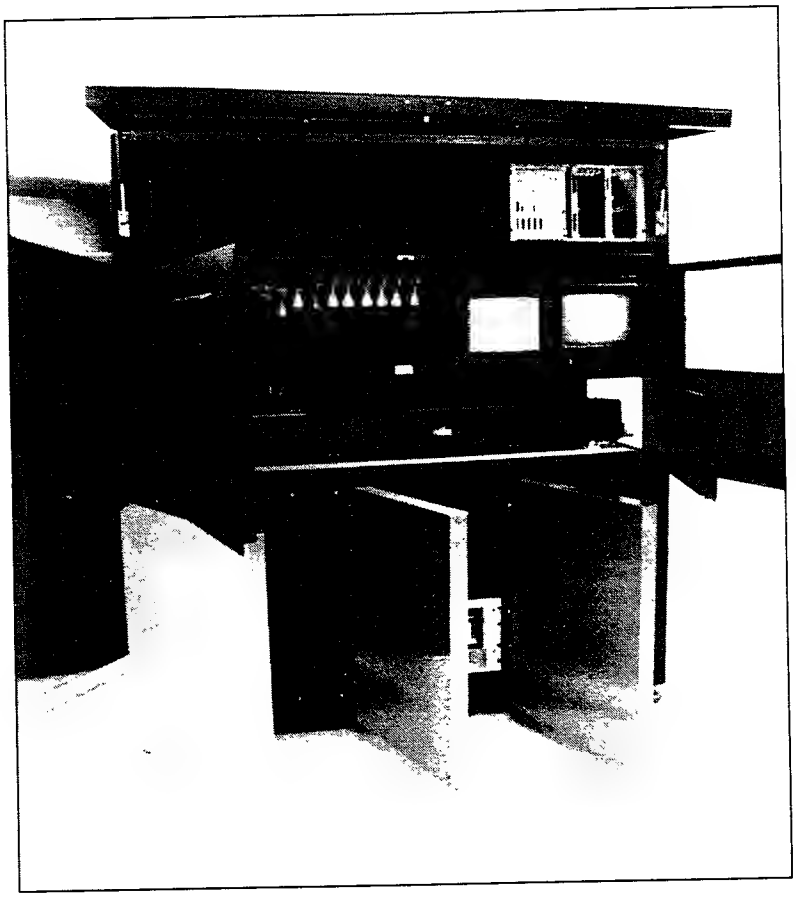
A typical chip dispensing machine is shown in Figure 1.6.1.4-3. This is the LASA laser pantograph. It is essentially a cluster of systems that perform CAD, lithographic

Figure 1.1.6.4-2

STRUCTURAL CHANGES IN MANUFACTURING



processing, and metal deposition via CVD. It uses prepackaged and prewired gate-arrays, that have no upper metal patterns. A designer inputs the design into the CAD system. This system then derives the patterning that in turn drives a laser beam. The laser beam acts as a pantograph, writing and depositing metal on the upper chip surface.



Courtesy: LASA
2233-155

Figure 1.1.6.4-3
The LASA Laser Pantograph

Figure 1.6.1.4-4 depicts the expected quantity of factories and chip dispensing machines that may develop over the next ten to twenty years. As mentioned, memory houses and standard IC houses will grow in capacity while shrinking in quantity, ultimately becoming highly regulated political preserves, much as happened in transportation and agriculture. ASIC houses will peak in quantity in about five to ten years as the fabless design houses drive them to ever-higher capacity as well. Chip dispensing machines will be slow in developing, but will ultimately be good enough that a semiconductor specialist will not be needed, so they will gradually displace most other types of factories, including the middleman.

Figure 1.1.6.4-4

STRUCTURAL CHANGES IN FABLINE QUANTITY

Type of Factory	*Approximate Number of Factory Locations*		
	'88–'90	*'92–'98*	*'98–'08*
Memory	80	50	20†
Traditional IC	300	150	40†
True Foundries	5	20	40
ASIC Houses	200	250	100
Fabless Design Houses	50	500	50
Chip Dispensing Machines	<10	<100	>5000

†About 50% Political Preserves

1.1.7 Manufacturing Technology

This section describes the process steps used in manufacturing semiconductors. It begins with a description of the basic steps involved in manufacturing an integrated circuit. This is followed with descriptions of processes for leading edge MOS and Bipolar circuits.

Semiconductor Manufacturing Basics

A semiconductor manufacturing process can be compared to an auto manufacturing process. Several operations such as welding, metal bending, and painting are involved. The type of vehicle being manufactured dictates the sequence and number of operations. For example, a compact car would differ from a recreational vehicle. The same viewpoint pertains to the semiconductor manufacturing process. However, the number and types of processes are dictated by the building technology (MOS, bipolar, linear, etc.), and the complexity of the circuit.

The semiconductor manufacturing process uses several technologies or processes where raw materials are subjected to different physical and chemical treatments. These raw materials are converted into microchips containing up to 100,000 individual electronic components on a 1/4" square piece of material.

Earlier, the manufacturing process was compared to the building of a house. This comparison grouped the manufacturing process into four principal activities:

- Mask Making
- Wafer Making
- Wafer Processing
  (including inspection activities)
- Testing/Assembly/Packaging

All of these activities will be included in paragraphs that follow. However, the wafer processing activities will receive the greatest attention.

Raw silicon is first transformed into prefinished wafer slices at the wafer-making stage. Silicon is a readily available substance that is classified as a semiconductor. This means that it cannot conduct currents of electricity easily unless impurity elements—such as boron, arsenic or phosphorus—are introduced. This is the important electrical characteristic which makes it possible to process devices on a silicon surface. The end product of wafer-making is a blank wafer. As such, it is ready to begin its processing journey towards being transformed into a set of devices.

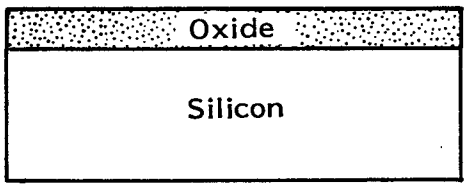
Preparation of the photomask set is an activity which must also take place before processing can begin. Photomasks are glass-like photographic plates used at successive stages in the processing of the wafer. When illuminated by a radiating source, they create images corresponding to the electrical elements of a circuit. Each circuit originates as a complex pattern of lines and rectangles. One mask is made for each of the photomasking steps in the process. There are many such pattern projection steps.

Using a computer, a configuration for each mask level is identified from the design composite and the digitized information stored on tape. A E-Beam mask writing tool, then takes this data and re-creates an identical pattern of lines, squares and rectangles on a photographic plate; only this time on a much smaller scale than the original. The single image of the circuit has now been placed on what is called a reticle. Reticles must be 100% defect free. A "defect free" reticle cannot have any pinholes, scratches, or other imperfections that could be copied later and cause devices to fail. Reticles can be used in a wafer stepper to expose wafers or they can be used in a step-and-repeat camera to make master masks. In this operation, a repetitive array of reticle images is produced on a photographic plate.

The overall array of images must be accurately placed onto the silicon so that all circuit elements or patterns will align to the previous photo-masking step. A typical MOS circuit will use about nine such masks. These must be aligned to within about 0.3 microns of each other. As a point of reference, a typical human hair is about 100 microns in diameter. So these masks must be utilized to an accuracy that is roughly equivalent to one three-thousandth of the diameter of a human hair. Such precision represents the capability limit of today's systems.

There are three basic operations involved in the wafer fabrication process. They are layering, patterning, and doping. Layering involves growing or depositing thin films of material on a wafer surface. Patterning removes selected portions of a layer so that only a desired pattern remains. Doping changes conductivity and resistivity of the wafer (substrate) material by placing impurities in selected portions of a wafer.

Let's follow a newly created wafer as it encounters each of the required masking steps in a basic MOS process. The process begins with first oxidation cycle. Wafers are loaded into a carrier called a boat which is then pushed into a high temperature furnace. Silicon will readily grow an oxide if exposed to oxygen in the air. To achieve the thickness required for device manufacturing in a reasonable amount of time it is necessary for the oxidation process to take place in a temperature range of 900°C to 1200°C. The oxidation process must yield a uniform, noncontaminated layer of silicon dioxide on the wafer. Figure 1.1.7-1 shows a wafer after initial oxidation.



Initial Oxidation

Figure 1.1.7-1

The wafer carrier is next moved to the photolithography area. The first step here is to coat the wafers with a photoresist. Photoresists are chemical mixtures that possess the property of changing their internal structure when exposed to various forms of energy, such as light, radiation or heat. They are like the coating on a photographic film. Wafers are coated by automatic resist-processing equipment, or "spin gear."

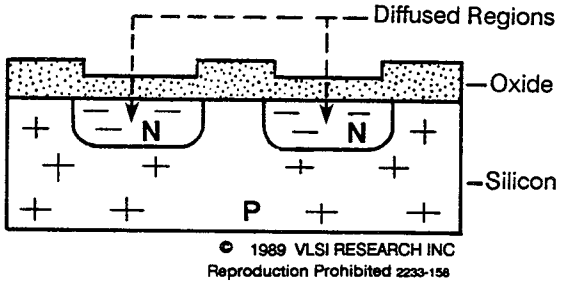
The wafers are now ready for the first of a number of photomasking operations. Photomasking is performed in an aligner. The aligner has two purposes at this step. First, there must be a precise alignment of the wafer with the mask. After alignment, light is radiated through the mask to expose the photoresist film on the wafer. The result of these two steps is the transfer of the mask pattern onto the photoresist.

Following alignment, the exposed wafers return to the resist processing equipment area where they are developed with chemicals. The process is very much like film development for a camera. All resist which was not protected from the light by the photomask is removed in the developing process. When using a "positive resist" development method, the coating remains only on those parts of the wafer which were not exposed to light. The wafers are then inspected through a microscope to see if the photographic patterns are satisfactory. After inspection, the wafers are baked in a small oven to make the imaged photoresist adhere properly.

Next, the oxide layer is removed in all places not directly under the remaining photoresist. This is done by a process called etching. Historically, this step was achieved with chemical etching procedures. Chemical ("wet") etching is the most economical and productive of all etching methods. There are two significant limits to this method, however. These are: accurate pattern placement and dimensional control limitations. This has lead to a newer "dry etchers" or "plasma etchers". Whatever the

method, the desired result is to etch away the oxide not covered by the photoresist.

The next step in the process is to remove the spent photoresist. This is done using "stripping" plasmas—or ashers—as they are sometimes called. Then the wafers are returned to the diffusion and oxidation area for a diffusion step in preparation for the next mask. Diffusion entails imbedding impurities into regions of the wafer where the base silicon has been exposed by etching. Elsewhere the oxide protects the silicon surface from diffusion. To do this, tiny particles of boron or other dopants are mixed with a carrier gas and the wafers are again loaded into a high temperature furnace. Gas then flows through the closed furnace tube. The impurities actually enter the silicon in much the same way that hot water absorbs tea particles. The wafers are once again etched to remove unwanted surface impurities and re-oxidized in a furnace to a specific thickness to cover the diffused regions. Figure 1.1.7-2 shows a wafer after the source/drain mask layer has been completed.



Source/Drain Mask

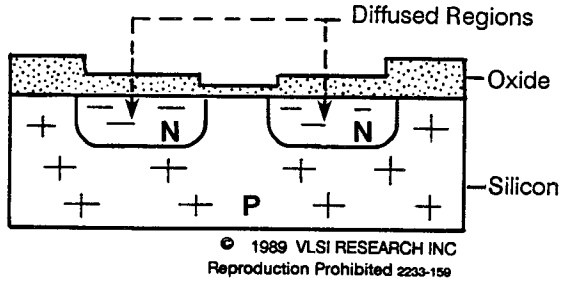
Figure 1.1.7-2

The wafers are moved to the photomasking area once again for reprocessing through the photolithography area. After photomasking, all the processing steps are repeated as before except that a new mask—the next in succession—is used to project the next pattern. The wafer then returns to the furnace where it will now go through a very special oxidation step. A wafer following the gate mask is shown in Figure 1.1.7-3. This is called the gate oxidation step. It is more critical than the previous oxidation steps, and is very carefully controlled.

The wafers are next sent to the ion implantation area. An ion implanter introduces impurities under the gate region. It works like a scaled-down atom smasher. Here the impurity elements—again, boron, phosphorus or arsenic—are ionized by using an electric arc and then accelerated through hundreds of volts, and directed so as to bombard the wafer at great speeds. The ions penetrate through the oxide and the upper layers of the silicon itself. This changes the conductivity of the silicon and renders some areas more conductive than others.

After ion implantation, the implanted wafers are annealed. The annealing process is used to correct stacking faults and dislocations of the silicon crystalline lattice. These damages occur during the various processing steps. In the past, annealing was done in annealing tubes. More recently, radiant lamp-flash annealers have been used.

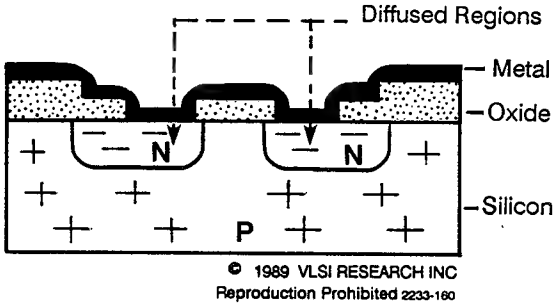
The wafers return once again to the photolithography area where they are coated, aligned to another mask, and developed. This mask defines the contact points where holes will be etched out from the unprotected portion of the wafer in order to allow contact with the outside world. This step is called metallization. At metallization the aluminum wires or other conductors are placed on the wafer by evaporation. This process is called deposition. This type of equipment has, therefore, become known as



Gate Mask

Figure 1.1.7-3

deposition equipment. Metallization techniques have undergone improvements and evolution in response to the demands of the new, high density circuits. The mainstay of metal deposition techniques was vacuum evaporation. The deposition method which is now used is called sputtering. This technique offers superior film composition and thickness control, and has become the dominant deposition method. These two different methods are similar in construction and operation. The process involves heating a metal in a vacuum so that molecules actually boil off and vaporize. The wafers are rotating within a bell-shaped chamber while the vaporized molecules are impinging on each of the wafers. The process is allowed to continue until the whole surface of the wafer is covered with a thin layer of metal, in this case aluminum, as shown in Figure 1.1.7-4.

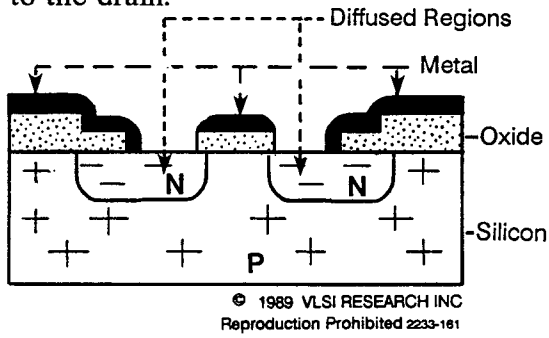


Contact Mask

Figure 1.1.7-4

The wafer goes through another photomasking and etching step which eliminates unwanted metal and forms the interconnecting wires, as shown in Figure 1.1.7-5. After etch the wafers are cleaned and inspected for satisfactory metal patterns. The wafers are then annealed in an oven to securely bond the metal to the oxide surface of the wafers. At this point, the wafers are almost completely processed. It is now necessary to protect the circuitry on the wafer against dirt and moisture. To do this, the wafers are placed in a atmospheric CVD reactor which coats them with a thin layer of glass.

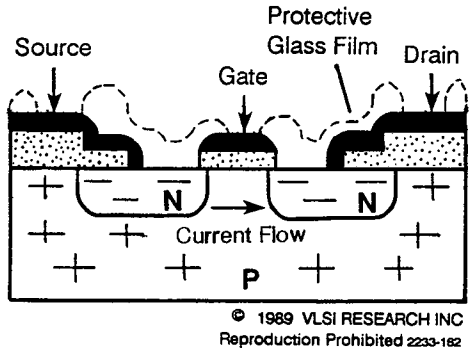
The wafers are now permanently protected from the environment. It is only necessary to remove the protective glass film from very small areas around the edge of each circuit. These areas are called "pads," to which wires will be attached during assembly. There are three 'pads' in an MOS transistor. They are called the source, gate, and drain, as shown in Figure 1.1.7-6. When the gate is charged above a certain threshold, current is allowed to flow from the source to the drain.



Metal Mask

Figure 1.1.7-5

After wafer fabrication, the wafer will be tested and then separated into individual chips, mounted and connected to a package. This part of the processing is called assembly. A sizeable percentage of the chips on a wafer will be defective, so it would be wasteful to assemble them. Identification of the good chips is the first step in test. It is done at wafer sort.



Silox Mask

Figure 1.1.7-6

For this test, the wafer is mounted on a flat vacuum chuck and each pad on the die is contacted by series of metal probes. The test is computer directed and may take from one second to several minutes. Non-functioning or out-of-spec circuits are auto-

matically marked by the tester with a drop of ink or on a computer map of the wafer. The bad dice will not be assembled.

As many as 75% of the masking levels in state-of-the-art devices are critical, i.e., critical in registration tolerance and/or dimension. In general, there are five to eight critical mask steps for a device, depending on the number of polysilicon/metal layers.

Today's state-of-the-art devices are fabricated with minimum feature sizes of one micron or lower. Device scaling rules dictate that film thickness decreases along with linewidth dimensions. As these dimensions decrease to even lower values, process steps will require equipment with advanced features and capabilities. In addition, process changes will affect the trends in equipment markets and sales. Equipment suppliers must be aware of these processes in order to react quickly to the changing requirements of advanced IC devices.

Advanced MOS Processes

Table 1.1.7-7 lists a typical one to two micron, dual poly parent process for both NMOS and CMOS. This is a leading edge process design and would be one of the more complex MOS processes encountered in the industry.

Most variants of this process will be subsets of these steps with some variations in their positioning. The descriptive processes on two layer metallization which are presented in the bipolar section are equally applicable here for a two layer MOS process. Epi deposition requirements as pertaining to MOS can be found in the bipolar section.

1 WELL OXIDATION

Equipment Required: Diffusion Furnace
Cleaning Equipment

Well oxidation is the first processing step a CMOS wafer receives in the processing plant. The wafer has been delivered to the user to his specifications by the silicon supplier. The mechanical, crystalline, and chemical conditions as well as the surface and bulk cleanliness of the wafer is part of the specification. Wafers are typically shipped in sealed trays or canisters with an inert, and often pressurized, atmosphere. Precleans, when they are employed, are wet and involve a standard procedure known as Standard Clean One (SC1), a water rinse, a Standard Clean Two (SC2), another water rinse, and finally a hydrofluoric acid dip followed by a rinse and dry. This clean takes place immediately before furnace loading.

Well oxidation is normally a straightforwardCMOS process step with no special requirements. Additionally, typical NMOS process might have a diffusion furnace step at this point to establish a denuded zone within the wafer if controlled oxygen content wafers are being used. This would be a lengthy high temperature process. Oxide thicknesses range between 2000-5000 angstroms. Tempatures of 1050°C are used, for times that can be as long as 24 hours. Tube load sizes can vary from 100 to 200 wafers.

Nitrogen and oxygen gases are used during thermal oxidation processes. Nitrogen provides an inert atmosphere for loading and unloading. Oxygen, the reacting element, is either provided directly as gaseous oxygen or in the form of steam. Wet oxidation offers an order of magnitude increase in oxidation rates over dry oxidation at the same temperatures. Steam may be generated by 'bubbler', 'flash', or 'torch' techniques. The latter, employing the combustion of oxygen and hydrogen, is believed to be the 'cleanest' from the standpoint of maintaining a closed system.

The major concern with the purity of house gases (N_2, O, and H_2) used at this operation is removal of metallics. This is prompted by the exposure of total bare silicon to these gases at this step. Mechanical filtration to 0.2 microns is frequently employed at point

TABLE 1.1.7-7

A TYPICAL LEADING EDGE MOS PROCESS

STEP	USAGE		PROCESS STEPS	EQUIPMENT REQUIRED
	CMOS	NMOS		
1	X	X	Well Oxidation	Diffusion Furnace, Cleaning Equipment
2	X		Well Mask	Aligner, Oven, Resist Process Equipment
3	X		Well Etch	Wet Etch Equipment, Rinser/Driers
4	X		Well Implant	Low/Medium Current Implanter
5	X		Well Drive	Diffusion Furnace, Cleaning Equipment
6	X	X	Initial Oxidation	Diffusion Furnace, Cleaning Equipment
7	X	X	Nitride Deposition	LPCVD Equipment, Scrubbers, Ultrasonic
8	X	X	Source/Drain Mask	Steppers, CD Measure Equipment, etc.
9	X	X	Nitride Etch	Plasma Etchers/Strippers
10	X	X	Mask Implant	Low/Medium Current Implanter
11	X	X	Punchthrough/Code Implant	High Energy/++Ion Implanter
12	X	X	Oxidation	Diffusion Furnace, Cleaning Equipment
13	X	X	Nitride Strip	Plasma Etch, Wet Etch Equipment
14		X	Depletion Mask	Aligner, Oven, Resist Process Equipment
15		X	Depletion Implant	Low/Medium Current Implanter
16	X	X	Gate Preclean	Wet Processing Equipment, Rinser/Driers
17	X	X	Gate Ox./Tunnel Oxides	Diffusion Furnace, Rapid Thermal Processor
18	X	X	Enhancement Implant	Low/Medium Current Implanter
19	X	X	Polysilicon Deposition	LPCVD Equipment, Scrubbers, Ultrasonic
20	X	X	Polysilicon Doping	Diffusion Furnace/High Current Implanter
21	X	X	Silicide Deposition	LPCVD or Sputter/Evaporation Equipment
22	X	X	Gate Mask	Steppers, CD Measure Equipment, etc.
23	X	X	Gate Etch	Plasma Etch Equipment
24	X	X	N+ Mask	Aligner,Resist Stabilization Equipment, etc.
25	X	X	N+ Implant	High Current Implanter
26	X	X	Resist Strip	Plasma Stripper, Wet Clean Equipment
27	X	X	Implant Activation	Diffusion Furnace, Rapid Thermal Processor
28	X		P+ Mask	Align, Resist Stabilization Equipment, etc.
29	X		P+ Implant	High Current Implanter
30	X	X	Oxidation/Oxide Deposition	Diffusion Furnace/CVD System
31	X	X	2nd Polysilicon Deposition	LPCVD Equipment, Scrubbers, Ultrasonic
32	X	X	Resistor Implant	Medium Current Implanter
33	X	X	2nd Gate Mask/Etch	See Gate Mask/Gate Etch
34	X	X	Oxidation/Oxide Deposition	Diffusion Furnace/CVD System
35	X	X	Doped Oxide Deposition	APCVD or LPCVD System
36	X	X	Reflow/Densification	Diffusion Furnace, Rapid Thermal Processor
37	X		Wafer Gettering	Diffusion Furnace, High Current Implanter
38	X	X	Contact Mask	Steppers, CD Measure Equipment, etc.
39	X	X	Contact Oxide Etch	Plasma Etch & Resist Stabilization Equipment
40	X	X	Reflow	Diffusion Furnace, Rapid Thermal Processor
41	X	X	Metal Deposition	Sputtering Equipment
42	X	X	Metal Mask	Steppers, ARC Spin Equipment, etc.
43	X	X	Metal Etch	Plasma Etch & Resist Stabilization Equipment
44	X	X	Alloy	Diffusion Furnace, Rapid Thermal Processor
45	X	X	Passivation Deposition	CVD Equipment
46	X	X	Pad Mask	Aligner
47	X	X	Pad Etch	Wet Etcher

of use to minimize metallic particles from gas delivery systems.

2 WELL MASK

Equipment Required: Aligner, Oven, Resist Process Inspection Equipment

This is the first mask a CMOS processes. This step must be done with the best overall locating accuracy and repeatability from wafer to wafer so that subsequent steps require minimal coarse alignment or operator intervention in the case of automatic alignment. Generally, resist dimensions are not extremely critical. This layer is relatively insensitive to particles, but very sensitive to resist pinholes. Even though this mask level is less susceptible than are others to particulate contamination, practice dictates that the masking line be operated at a level of cleanliness consistent with the most critical level processed.

Cleanliness of photolithography operations is important at all mask levels. They will be discussed here and referred to in descriptions of subsequent mask steps. Photoresist, as delivered, is specified to some predetermined purity level. The specification is generally of vendor origin. Still, it reflects the requirements of a major segment of users. Historically, relevant resist properties have been its particulate content, viscosity, specific gravity, water content, flash point, metal content, refractive index, haze and surface tension, to name just a few. However, in recent years, resists and developers have come to be regarded as potential sources of contamination. Their principal contribution to contamination is particles of sodium and metallic ions.

Regardless of the specified limits of particles in resists, users are moving towards additional point-of-use filtration. The objective is to remove incoming particles, and particles created or introduced in the opening, closing, and replenishing of the resist dispense system. Point-of-use filtration also aids in the removal of colloidal particles that form with time in the resist. Resist filtration to 0.2 microns, or less, is normally used on lines working with 3 micron or less geometries.

Other cited sources of particulate contamination in photolithography areas are cassettes, resist wafer track systems and wafer handling systems associated with aligners. Cleaning of tracks and handling systems is performed manually using a variety of solvents, surfactants, and commercially available lint free wipers. Edge-rounded wafers reduce the incidence of silicon chips but wafer breakage can and does occur. Specialized vacuum cleaners and plumbed house vacuum is required.

Historically, the wafer has also been inspected for particulates in the course of photoresist develop-inspect. But a 100% wafer inspect is seldom used now. On many lines photoresist develop-inspect has been discontinued or is limited to the measurement of a critical dimension on a sampled wafer. The majority of process control problems requiring 100% inspection have now been solved on most product lines. This, coupled with the added exposure to ambient contaminants in the course of inspection, has lead to lot-acceptance on a sample wafer basis.

Most modern lines susceptible to particulates will monitor and have the process qualified on the basis of periodic test wafers. A blank oxidized test wafer that is processed alongside patterned wafers will be inspected for particles and for particle density. The particle density will be recorded. The wafers will then be resist-coated, aligned, exposed, and developed. The test wafer will be inspected once again for particle density. Any increase in particle density is then due to the process step. Specific sources of interest, whether they be equipment or materials, can then be further isolated by exposing the test wafer to them and measuring the increase in particles.

Most sophisticated product lines have standards of measurement for particles. Sizes of particles deemed damaging to photolitho-

graphy patterns are a function of the minimum line width, or spacing, of the patterns. Photolithography damage is of concern when these particle sizes approach 25% to 30% of minimum line widths. Measurement of particles equal to or greater than 0.5 micron is a prevalent practice. Achieving particle densities of 0.5 particles/cm^2 is the current level of activity for most 3 micron lines. Many would like to achieve an order of magnitude improvement in particle density down to 0.05 particles per square centimeter. Those working with smaller feature sizes cite equivalent densities for particles of 0.3 microns or greater. Particle counting by microscope is too laborious and too subjective for this type of monitoring. Product lines needing this precision usually employ one of the automated surface particle counters such as that offered by Aeronca, Hamamatsu or Tencor. Practitioners of this method also commonly requalify the photolithography line at the start of each day.

3 WELL ETCH

Equipment Required: Wet Etch Equipment
Rinser/Driers

Etching of the wells for this mask level can be performed equally well by wet or dry techniques. Newer designs often require plasma etchers with high selectivity oxide etch processes. High density CMOS devices at linewidths of below 1.5 microns will require dry processing using a SF_6 plasma. Normally, well mask etch is a wet process.

Oxide wet etchants are universally composed of hydrofluoric acid (HF) buffered with ammonium fluoride (NH_3F). This buffered oxide etch (termed BOE) is typically formulated in a ratio of 1:8, HF:N-H F, although other formulations are used. A wetting agent is frequently added. Most product lines use premixed BOE purchased commercially. Particulate and metallic ion content control is critical. The etching is done by immersion in BOE, followed by a rinse/dry. Wet oxide etching is usually segregated by application. One station is usually allocated to undoped strata, such as initial and gate oxides. One or more separate stations are used for doped oxides. This prevents cross contamination by released dopant ions.

Resist stripping may be either wet or dry. At this step, the resist has not yet been subjected to high current implants or to planar-plasmas. Consequently, very highly cross-linked polymers are not usually present. In this case, a wet only strip is effective.

4 WELL IMPLANT

Equipment Required: Medium Current Implanter

This step provides the dopant for CMOS well regions. Dopants of B+ or P+ at low to medium dose levels of 1E12-1E13 and energies of 120 KeV. Absolute value of the implant dose and uniformity are critical to establishing good threshold control on the finished product. In more exotic processes this step may consist of multiple implants of varying doses and energies to create special profiles.

Thin oxides (500Å) are often provided over intended areas of implant. The intent, in part, is to protect exposed silicon. Originally, these oxides were deposited. It is now believed that natural thin oxides resulting from ambient exposure are adequate. Theoretically, only those ions which have been appropriately extracted and accelerated by the ion-implant equipment will have gained sufficient energy to penetrate this oxide and reach the silicon. The thicker initial oxide remaining from the well mask step will block all other unwanted ions.

This finished well region will overlay the deepest junction formed in a CMOS circuit. It is thus desirable to implant the ions as deeply as possible to minimize requirements for thermal diffusion. There is a trend towards higher energies to achieve this result. Higher energies, however, are also more capable of ionizing unwanted con-

taminants in the systems and contaminating the wafer. Users of implant systems are therefore looking more at problems caused by equipment–sourced contamination at ion-implantation.

5 WELL DRIVE-IN

Equipment Required: Diffusion Furnace
Cleaning Equipment

This drive-in activates the preceding implant and establishes a deeply diffused well to accommodate the complementary devices used in CMOS. It is typically a diffusion furnace operation, and it is also the highest temperature–of longest duration–that the wafer will ever be submitted to. Temperatures approach 1200°C. Furnace times often exceed twelve hours. Consequently, ionic contamination that is either already present or that is introduced in the course of this operation will be thermally diffused as well. Consequently, pre-cleans are used universally. They usually consist of hydrofluoric acid dips, with attendant rinsing and drying.

This drive-in step receives a high degree of attention with regard to chemical, gaseous, and ambient contamination. Frequently, polysilicon or silicon carbide tubes will be used in lieu of quartz. The former materials provide a barrier to contaminants that may be given off by furnace heating coils and other tube exterior sources. An alternative method consists of using a double walled quartz tube. Gaseous HCl is passed through the annular spaces separating the inner and outer tube.

House nitrogen and oxygen for the tubes is filtered to 0.2 microns at the furnace itself using point-of-use filter. Mobile ion contaminants are monitored by C-V techniques. Acceptable drifts are 0.1 to 0.25V, depending on the product line.

6 INITIAL OXIDATION

Equipment Required: Diffusion Furnace
Cleaning Equipment

This is the first processing step employed on NMOS product lines. Here, clean considerations are identical to those used at Step 1, on CMOS lines.

For NMOS processes, this step is universally performed by a thermal oxidation. It provides an oxide of approximately 5000 Å thickness. The oxide will be later patterned and be used to differentiate circuit, field and active device areas.

CMOS lines also employ a thermal oxidation for the same purpose. In the case of CMOS, the wafer is stripped to bare silicon prior to oxide growth. This is done, in part, to remove doped oxides that may have occurred through thermal doping or well drive and to re-approximate a planar surface. Unfortunately, the total silicon surface of the wafer is then exposed to contaminants just prior to a high temperature operation. The oxide is stripped in dilute HF followed by a brief rinse-and-dry cycle.

While furnace temperatures and times are lower than those used at CMOS well drive-in, the same considerations for high purity, low particulate chemicals and gases prevail for both processes. Lower temperatures allow the use of quartz tubes, but periodic capacitive-voltage checks of tube condition are performed as well. Drift limits are typically 0.25V.

7 NITRIDE DEPOSITION

Equipment Required: PECVD Equipment
Ultrasonic Scrubbers

Nitride deposition for any MOS process is extremely sensitive to particulate contamination. Contamination within or under the

film is catastrophic and particles on top of the film must be removed with scrubbers or ultrasonic cleaners. Thickness control is also critical to avoid color variation in the composite of nitride and initial oxide which can affect exposure and dimensional control at the next masking step.

The silicon-nitride deposition reaction requires silicon-bearing and nitrogen-bearing gases. These are typically dichlorosilane or silane and ammonia. These gases, as well as purge gases, should be free of oxygen, moisture and metallics. Oxygen reacts more readily with silicon than does nitrogen. Hence, the system is very susceptible to leak contamination.

Inspection procedures typically call for observing one or two products or one or two test wafers per pass. This is done under high intensity collimated light. Inspection seeks to identify a haze or particles. Laser surface particle detectors are being used more widely in conjunction with test wafers to monitor or qualify operation cleanliness.

In addition to these preventive measures, a post-deposition scrub is frequently employed also. This may occur at a scrub station in the films area or—less frequently—in the masking area just prior to resist application.

8 SOURCE-DRAIN MASK

Equipment Required: Steppers, CD Measure Equipment, etc.

This mask delineates the source and drains of all active devices. It also includes those areas that will ultimately be masked to establish gate regions. Dimensional control and resolution control parameters are more stringent here than they were in the previously-discussed well-mask. Particulates can cause etched pinholes in the areas destined to be gate regions. This can result in an undesirable localized field implant in device's active channel region. The affected device's and circuit's electrical characteristics would be altered, thereby rendering the device inoperative. Typical CD measurements are shown in Figure 1.1.7-8. Steppers are generally required. They are needed to meet the exposure control criteria and tight control over all developer parameters is also necessary to achieve adequate repeatability.

9 NITRIDE ETCH

Equipment Required: Plasma Etchers/Strippers

The prior source-drain mask is designed to protect the source-drain regions and expose the field to this etching step. Etching may be either wet or dry, but plasma etching is now prevalent and will remain so. Barrel or planar type plasma etchers may be used, with a trend towards planar machines. Selectivity to oxide as well as etch uniformity are the major criteria driving equipment selection. A CF_4 or comparable gas is used to provide the F-reacting species. A variety of fluorine-bearing gases are available and are being developed with application specific properties.

10 MASK IMPLANT

Equipment Required: Medium Current Implanter

The mask implant step can be either a field implant for CMOS or an enhancement implant for NMOS at this point in the process. This step is usually an oversize mask to block an implant. Cleanliness and freedom from pinholes are crucial to avoid blocked implants or unwanted implanted areas. Implants vary over a broad range of energies depending on the process. They are frequently in a dose range of 1E13-1E14 B+ or BF , at 30KeV.

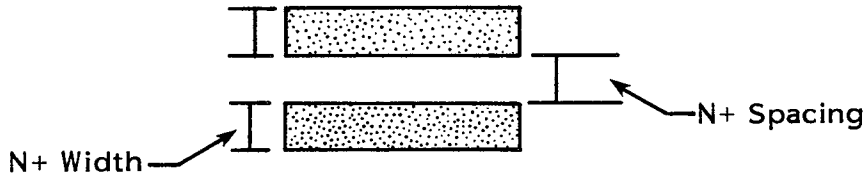
11 PUNCHTHROUGH or CODE IMPLANT

Equipment Required: High Energy Ion Implanter

The punch through implant is generally high energy and may employ a doubly ionized species. This is a low to moderate dose

Figure 1.1.7-8

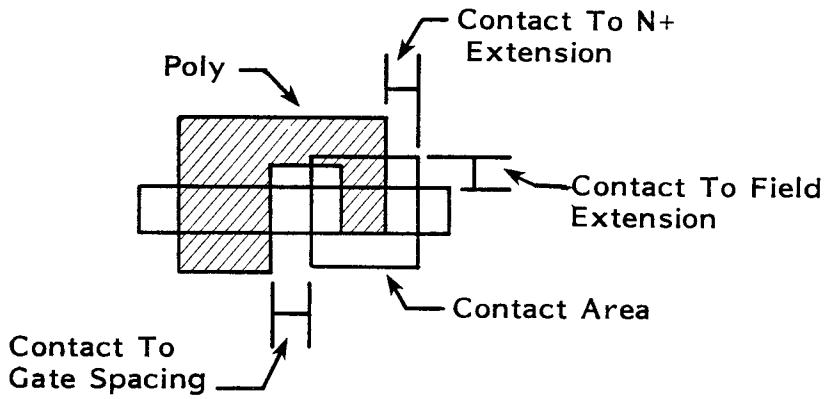
Source-Drain Mask Critical Dimensions



TYPICAL MEASUREMENTS
(in microns)

Linewidth	1.0	1.5	2.0
N+ Width	1.1	1.7	2.2
N+ Spacing	1.3	2.0	2.6

Gate Mask Critical Dimensions



TYPICAL MEASUREMENTS
(in microns)

Linewidth	1.0	1.5	2.0
Contact To N+ Extension	0.4	0.6	0.9
Contact To Field Extension	0.3	0.4	0.6
Contact Area	0.9	1.4	1.8
Contact To Gate Spacing	0.7	1.1	1.4

implant, 1E11-1E13, B++, at >150KeV. It is designed to prevent subsurface leakage currents for high voltage devices. A similar implant may be used for ROM encoding. Here, an encoding resist layer exposes selected gates to implantation. Devices so implanted cannot be turned on.

This implant may replace Step 10 or be employed elsewhere in the process. The contamination criteria remains the same. Blocked or unwanted implants will have a major yield impact.

12 FIELD OXIDATION

Equipment Required: Diffusion Furnace
Cleaning Equipment

This step, when used, is preceded by complete removal of any prior photoresist. Wet or dry removal methods may be used. This oxidation is somewhat less critical, in that, active source-drain regions are protected by silicon-nitride. Field oxidations are usually non-critical operations have moderately broad thickness and uniformity specifications. Current thicknesses are 0.7-1.2 microns deposited at 1000°C. The wafers are often cleaned with the typical hydrofluoric acid, D.I. rinse cleaning techniques series. The oxidation tube is also monitored with C-V wafers. Drift criteria may be somewhat relaxed (0.5V). Tube cleaning is as discussed previously.

13 NITRIDE STRIP

Equipment Required: Plasma Etch
Wet Etch Equipment

The nitride film over the source-drain areas is removed by a plasma etch (SF_6), or by a wet acid etch (hot phosphoric). Wet etching predominates because there are no geometrical considerations. The etchant used is hot, typically in excess of 170°C. The etch is followed by a D.I. quench and a rinse-dry. Plasma will etch the underlying initial oxide, although the rate is less than for the overlying nitride.

14 DEPLETION MASK

Equipment Required: Aligner
Resist Process Equipment

This step is an oversize mask designed to expose depletion load gate regions for the depletion implant. Cleanliness and freedom from pinholes are crucial to avoid blocked implants or unwanted implanted areas. This is a non-critical alignment. Overlay requirements are '0.8-1.25 microns. This masking step is used only for NMOS and thus will see decreased usage as IC manufacturers move toward CMOS.

15 DEPLETION IMPLANT

Equipment Required:
Low/Medium Current Implanter

Normally this is a low to medium dose implant (120KeV) used primarily in NMOS processes with P+ at 1E12-1E13 as the dopant species. Uniformity and dose control are critical to maintain adequate device threshold voltage control. As with other steps exclusive to NMOS, decreased production of these devices will impact equipment suppliers.

16 GATE PRECLEAN

Equipment Required: Wet Processing Equipment
Rinser/Driers

The preclean prior to gate oxidation usually includes an HF dip. This is done to remove all oxide in the region where the gate oxide is to be grown. This step exposes bare silicon to possible contamination. Sources include metallic compounds which affect the device electrically and particulates which can cause pinholes in the gate oxide. Consequently special low-particulate, ultra-pure chemicals and filtered etch baths are normally required for this step.

17 GATE OXIDATION/ TUNNEL OXIDES

Equipment Required: Diffusion Furnace
Rapid Thermal Processor

Gate oxidations are almost always grown in a furnace tube. They require that furnaces be ultra clean from particulates. This step may use either low temperature wet oxidations or higher temperature dry oxidations. Sometimes HCL is added to provide metallic contamination gettering. In all cases thickness control and uniformity is paramount in today's high density processes. Rapid thermal annealers are beginning to play an important role as oxides grow thinner as a result of device scaling. They already have applications in EEPROM's. Most EEPROM manufacturers use very thin (< 10 nm) tunnel oxides. Diffusion furnaces can't be used because of ramp rate limitations with high thermal mass furnaces.

18 ENHANCEMENT IMPLANT

Equipment Required:
Low/Medium Current Implanter

CMOS processes frequently employ this step earlier in the process, usually following a depletion implant. NMOS and some CMOS processes adjust enhancement device thresholds at this point. Cleanliness considerations cited in the prior depletion implant are even more critical here. Dosage levels are relatively low, 1-5x10 ions/ cm^2, B+. 'Blocking' by particles decidedly affects device thresholds and consequently, circuit performance and yields.

Dosage level and uniformity is difficult to monitor at these low levels this early in the process. Uniformity, in all cases, is limited by the size of the capacitive-voltage structures used in the measurements. Localized blocking in the smaller areas 'shadowed' by particles cannot be site-identified. This type of problem is only detected after completion of processing and subsequent yield analysis.

19 POLYSILICON DEPOSITION

Equipment Required: LPCVD Equipment
Scrubbers, Ultrasonic

The Polysilicon that is deposited at this step will be subsequently masked to form the gate electrode and to provide a small portion of the interconnect busing. The poly is deposited by chemical vapor deposition. Particulate contamination is a major problem at this step.

Those generic problems associated with CVD equipment, as were discussed in Nitride Deposition at Step 17, apply here as well. Tube cleaning is typically required every 20-40 passes, while the easier boat cleaning may occur more frequently at every 20 passes.

Precleaning is avoided. Upon leaving gate oxidation, the wafer is as clean as can be achieved on today's product lines. The wafers are off-loaded from the oxidation boat directly onto the LPCVD boat. Those product lines with intervening enhancement implants will typically employ a hydrofuoric acid clean after resist strip.

As is the case with the previously-described stoichiometric nitride deposition, particulates can create nucleation sites on the wafer and within the reaction chamber. Dendritic and nodular structures can form on these surfaces. Small submicron particles can cause significant line width distortions. A high density of these structures on the wafer surface may require a post deposition 'scrub' clean to effect their removal.

The stoichiometry of the process is somewhat less critical than it is with nitride. Notwithstanding, a relatively high degree of purity is required in the silicon-bearing silane and the carrier gases. Gases should be free of oxygen, moisture, transition metals and heavy metals. Additional filtration is employed at the point of delivery to

the equipment to remove potential contaminating particles that may have been resident in the house-gas delivery system.

Thickness and uniformity are obviously critical parameters. Grain size control and orientation is also a dominant factor in most of the two layer poly processes. This is critical to growing good quality thermal oxide on top of the poly layer. Small grain sizes, <1000 angstrom, are also desirable to improve line edge definition when the poly is patterned. Grain size control can be obtained by proper control of temperature and gas flow. Film thicknesses are in the 2000-5000 angstrom range. Silane gas is used to deposit the film.

Several wafers from each lot are typically examined by the naked eye, under UV or collimated light, at loading and unloading. The observed film should be free of haze and particulates. More stringent product lines have successfully used automatic surface scanners on test wafers to periodically monitor and qualify this process step.

20 POLYSILICON DOPING

Equipment Required: Diffusion Furnace
High Current Implanter

The purpose of this doping step is to convert the already deposited polysilicon into a conductive material. Doping may be accomplished by a furnace predeposition or by a high current implant. Furnace-deposited phosphorus is the more prevalent. Furnace predeposition would require an HF dip preclean cycle as well as a post deposition 10:1 HF deglaze. Implantation using arsine is an alternative for devices with thinner Polyfilm thicknesses. Implantation does require a subsequent drive-in. Here the advantage is that arsenic-doped polysilicon outgases less than does phosphorus and is less likely to cause subsequent autodoping.

Careful activation of the implant must be done to avoid edge profile problems at poly etch. This is due to different plasma etch rates between amorphous and polycrystaline silicon. With either dopant technique, thermal processing must be tailored to minimize grain growth which could cause edge definition problems at gate mask. Rapid thermal annealers are advantageous in minimizing grain growth.

This step is not as susceptible to contamination as are most other operations. Uniform polysilicon sheet resistance is required to a typical uniformity of '5%. It is not a parameter that is easily affected by particle blocking in an ion-implanter.

Susceptibility to ionic contamination becomes of concern at elevated temperatures. This is an additional reason for the increasing trend towards implantation methods, rather than furnace methods for this step.

21 SILICIDE DEPOSITION

Equipment Required: LPCVD or PVD

This optional step is used for high speed circuits or where designs require long, polysilicon, signal buses. The deposition of refractory metal silicides greatly increases effective sheet conductivity of the underlying polysilicon layer. Tungsten and molybdenum silicides are the most commonly used. Tungsten silicides are generally formed by chemical vapor deposition. Molybdenum silicides are formed via sputtering methods. Uniform film composition and internal stresses within these films require tight control. Oxygen, nitrogen, and carbon are potential contaminants if they are present during the reaction.

Films must be uniform in thickness and resistivity to be useful. Film stress, composition, purity, and adhesion to underlying layers are also extremely important. This step may require additional constraints on both pre-deposition and post-deposition processing steps up to the end of the process. This is because deposition parameters are so tight. Both deposition methods result in poor compositional control, large volume shrinkage and high stresses. Stress

is lowered by the use of an annealing step. Sputtering techniques suffer from incorporation of oxygen and carbon in silicide films while marginal step coverage is obtained in evaporated films. Although co-sputtering from individual targets of refractory metal and silicon targets improves compositional control, film properties are difficult to control and are plagued by the above PVD problems. CVD films are limited to tungsten. However, they produce highly pure, reproducible films with good compositional control, step coverage and adhesion.

Both chemical vapor deposition equipment and sputtering equipment suffer from deposited material buildup on reaction chamber walls. Periodic equipment cleaning is required.

Source purity with regard to mobile ions is important to prevent their introduction. Wafer precleaning is limited to a dilute HF dip, a rinse, and a dry to remove any insulating oxide the polysilicon may have acquired. Sputtering systems equipped with biasing may remove these oxides by back bias sputter etching.

22 GATE MASK

Equipment Required: Steppers
CD Measure Equipment
Resist processing Equipment

The gate mask is typically the most difficult step in any MOS process. This is primarily due to the dimensional control requirements for the step. Additionally, there is difficulty in measuring the extremely small dimensions prior to etching the poly layer. Table 1.1.7-8 (shown previously) gives the CD measurements for this step. Resist thickness and uniformity is critical as well as alignment, exposure, and develop control. Reproducibility in the develop cycle is usually the key to success at this step. However, this is true only if steppers are used for pattern exposure. Processes using projection aligners must have good control over all aligner parameters which affect image contrast and resist profile. Otherwise, poor CD measurements can result. Softbake temperature and humidity levels can also affect dimensional control.

23 GATE ETCH

Equipment Required: Dry Etch Equipment

Processes must have a high degree of anisotropy and selectivity. Both freon and chlorine chemistries can be used for this step. Thinner gate oxide processes may require chlorine chemistry due to higher selectivity requirements. High selectivity is needed to achieve adequate gate oxide thickness after etch. Profile control is critical and depending on process requirements may vary from a 60 degree slope to a 90 degree vertical edge. Re-entrant profiles are not acceptable if more than a degree or two off dead vertical. Sufficient overetch time is needed to clear poly residue from steep steps and to slow fast etching areas. For example, undoped regions of poly resistors in a RAM process will etch faster than the doped poly. Dry etch equipment is used almost exclusively for most poly etch processes. Control of Radiation damage to the underlying gate oxide and preferential etching along grain boundaries are major factors in etch equipment selection. Resist hardening techniques such as PRIST are desirable to reduce resist loss and resulting CD changes during the etch.

24 N+ MASK

Equipment Required:
Aligner, Resist Stabilization Equipment, etc.

This step delineates the source-drain regions of those active devices which will be implanted to form the n-channel transistors. All devices on NMOS circuits will be implanted; approximately one half of the devices on CMOS circuits will be implanted. CMOS p-channel transistors will be formed somewhat later in the process.

This mask is oversized. It exposes the n-channel source and drain. The poly gate

formed at this point will block implantation of the underlying channel region. The main criteria at this step is to ensure that the resist will tolerate the high dose implant it will be exposed to. Deep UV resist stabilization or photomagnetic curing is desirable to minimize damage problems during the implant.

The mask is more critical for CMOS than it is for NMOS. Resist voids in the N+ dopants may be introduced into future p-channel regions. Particulate contaminants that will block N+ implants are of concern for both technologies. All preceding comments on photolithography hygiene apply.

25 N+ IMPLANT

Equipment Required: High Current Implanter

High dose 1E16 ions/cm^2 arsenic implants at 60KeV are typically used at this step. They usually create sufficient wafer heating to damage the surface of the resist mask. Wafer cooling is a must.

Ion implantation, using arsenic, is the predominant doping method. Principal contamination concerns are particulates on the surface, blocking implantation in localized unintended areas. Source purity of Arsine gas is most important because the implanted species will affect source and drain junction characteristics.

26 RESIST STRIP

Equipment Required: Plasma Stripper
Wet Clean Equipment

Removal of resist exposed to a high dose implant normally requires both a plasma oxygen strip followed by a wet chemical strip to remove any remaining residue prior to implant activation. The wet chemical clean can be done equally well in either a sink or a wet machine. Wet stripping of hardened resist will predominate even on VLSI devices. This is because only wet stripping removes metallic contaminants on the wafer surface.

27 IMPLANT ACTIVATION

Equipment Required: Diffusion Furnace
Rapid Thermal Processor

Activation of the implanted arsenic can be accomplished by either rapid thermal annealing or by diffusion tube drive-in. In NMOS, an oxide regrowth is required over source-drain regions at this point to re-establish planarity. Consequently, a combined furnace drive-in/oxidation is most common for NMOS. While drive-in times and temperatures are substantially less than those in Steps 5 and 6, the same cleanliness criteria and preventive measures are employed. CV drifts in excess of 0.25V usually initiate some corrective action.

28 P+ MASK

Equipment Required:
Align, Resist Stabilization Equipment etc.

These mask steps provide for the delineation and doping of the p-channel complementary devices. The main criteria at this step is to ensure that the resist will tolerate the high dose implant it will be exposed to. Deep UV resist stabilization is desirable to minimize damage problems during the implant. Cleanliness considerations are identical to those in Steps 24 and 25.

29 P+ IMPLANT

Equipment Required: High Current Implanter,
Stripper

This step is to dope the P-channel complementary devices. The doping level is high, between 1E14 and 1E16 ions/cm^2, boron. Low energy (<50KeV) with high current implant techniques are used. Particulate contamination, leading to implant blocking is of concern, as was the case with the prior N+ implant. There is usually sufficient wafer heating to damage the surface of the resist mask. Wafer cooling is a must at this step. A high energy silicon implant may be used. This is done to create amorphous layers prior to the boron implant. A silicon implant reduces the

tailing effect common to boron and produces shallower junctions. High currents are required to reduce implant times after this step. Once again, wafer heating and implant levels render resist removal more difficult than with other steps. A post-implant resist strip is required.

30 OXIDATION/OXIDE DEPOSITION

Equipment Required: Diffusion Furnace
CVD System
Wet Cleaning Equipment

CMOS wafers will arrive at this point from Step 29, but NMOS wafers may arrive from Step 27. NMOS wafers that were already activated via the combined furnace drive-in/oxidation would bypass this operation. All CMOS wafers, however, arrive from a step employing photoresist as a high current implant mask. The resist has been previously stripped at the masking or implant resist strip station. Notwithstanding, an additional oxidation pre-clean is employed for any and all wafers at this step.

Generally a thermal oxide of the poly and a LTO CVD oxide is used at this point in the process. It is used to protect the source/-drain regions from any deposited doped oxides and to act as an insulator or gate between the first and second poly layers for the capacitor on DRAM cells. When this layer is deposited with a CVD system it is followed by a furnace densification. In either case, oxide thickness and uniformity are critical parameters. This oxide layer is typically 500-3000 angstroms thick.

31 SECOND POLYSILICON DEPOSITION

Equipment Required: LPCVD Equipment
Ultrasonic Scrubbers

A second level of polysilicon is commonly used for DRAM's and other high density devices. It can offer the advantages of 'building in' capacitors where they may prove electrically advantageous as well as providing an additional level of interconnection. Another application is creation of on-chip high resistance—and relatively precise—polysilicon resistors. All the considerations of Step 19, the first polysilicon layer, apply here.

If 2nd poly is used, Steps 32 through 35 are required.

32 RESISTOR IMPLANT

Equipment Required: Medium Current Implanter
Scrubber

This step is used to dope the second polysilicon layer; ion implantion is normally used. A 'resister' implant is typically used for some static NMOS RAMS. Here, a light dose (1E13 to 1E14 ions/cm^2) leaves the polysilicon with a relatively high sheet resistance. Other applications, where the silicon is used as a conductor will employ higher doses. In any event, the 2nd poly receives a 'blanket' implant over the entire wafer so no masking is used. Precleans are not normally used. Where the prior 2nd poly has accumulated particulates, a post poly deposition 'scrub' may be used.

Implant dose and uniformity cannot be measured on product wafers at this point. Separate blank test wafers may be employed and measured by CV techniques.

33 2ND GATE MASK/ETCH

Equipment Required: Stepper, Inspection
Etcher, Stripper

Gate mask, while the common terminology used here, may be a misnomer. The resulting poly lines do not delineate subsequent doping and diffusion operations. Dimensional control is less critical than it is in Step 22, but it is still a concern. Particulates are undesirable. Planar plasma etch is employed, followed by a dry-wet resist strip.

34 OXIDATION/OXIDE DEPOSITION

Equipment Required: Diffusion Furnace
CVD System
Wet Cleaning Equipment

This oxide provides part of the dielectric between the preceding polysilicon and subsequent aluminum. It may be formed by low temperature oxidation or by chemical vapor deposition methods. The oxide is thin (500-1000Å) and protects the underlying polysilicon from the subsequent doped oxide deposition. Particulate debris, silicon, quartz, and redeposits will degrade the dielectric and the dopant barrier properties. The tube is not normally CV plotted but does receive a scheduled clean every 6 months—on average.

Precleans are employed but are usually limited to a clean sulfuric-peroxide treatment followed by a rinse-dry. HF is not appropriate at this step due to the exposure of underlying oxide.

35 DOPED OXIDE DEPOSITION

Equipment Required: LPCVD
APCVD
Scrubber

This step increases the thickness of the previous oxide, from typical values of 500-1000Å to about one micron (10,000Å). The oxide is usually deposited by atmospheric or low pressure chemical vapor deposition methods. It is phosphorus and boron doped. Doping allows a more planar coverage when the oxide undergoes a subsequent thermal reflow step. In addition, the faster etch rates of the doped oxide, in conjunction with the slower etch rates of the underlying undoped oxide, can be used to slope contact openings.

Selected wafers from each lot are normally monitored for particulates under UV or high intensity light with the unaided eye. In addition, blank test wafers may be periodically run with the product with post deposition examination using a surface scanner. Should gross particulates appear on the wafer, a scrub clean may be employed as a 'salvage' measure, in lieu of scrapping.
On older product lines, and in the absence of 2nd poly, Steps 34 and 35 may be performed in the same reactor with a single pass. The oxide is initially deposited without doping and the dopant gas is then introduced later for the remaining thickness required.

Because CVD systems—on the whole—are susceptible to, and can also generate, contamination, the deposition of doped oxides poses further problems. Phosphorus 'enriched' particle sites also pose problems. Localized high phosphorus concentrations not only inhibit resist adherence, they also accelerate etching at a rate up to three times that of normal concentrations. Additionally, high phosphorus concentrations in the presence of moisture can be corrosive to aluminum. Consequently, the deposited oxide must be uniform in composition. Further, it must be amorphous so as to provide good dielectric between underlying polysilicon and the subsequent aluminum interconnect level.

All of these properties predicate a particulate-free wafer before and during this deposition. The wafer arrives from oxidation Steps 30 or 35. These steps usually result in a surface as clean as can be achieved by available cleaning methods. Precleaning is an option, depending on the product lines' ability to maintain clean transport and/or storage. Precleans, when employed, usually consist of a sulfuric- peroxide or hydrofluoric acid treatment followed by a rinse and dry.

Equipment redeposits are a major source of particulate contamination and frequent cleaning of chambers and wafer handling hardware is required. Cleaning frequency and methods are dependent on the equipment used. Atmospheric Pressure (APCVD), Low Pressure LPCVD) systems may be used. LPCVD is more common on newer lines in the United States. APCVD of arsenic doped glass is commonly used in Japan.

36 REFLOW/DENSIFICATION

Equipment Required: Diffusion Furnace

This step is used to planarize the surface of the doped oxide. This is necessary due to depth-of-focus limitations in aligners and step coverage limitations in sputtering systems. The layer is heated to its melting point and allowed to flow slightly. Ambients which reduce surface tension can improve the flow characteristics of the glass. This step also serves to increase the density of the oxide. Diffusion furnaces are typically used.

37 WAFER GETTERING

Equipment Required: Diffusion Furnace
High Current Implanter

This step is used by some CMOS product lines. It can occur either before or after the contact mask, depending on the process. It consists of a high dose phosphorus implant on the wafer backside, followed by a furnace anneal. The intent is to create backside damage sites and encourage the thermal migration of ionic contaminants to these capture sites. Ambients, times, and temperatures are critical parameters. This step is characteristic of CMOS technology. Nevertheless, the step is not critical and usually does not employ cleans.

38 CONTACT MASK

Equipment Required: Steppers
Resist Processing Equipment
CD Measure Equipment, etc.

Contact masking and etching is one of the most difficult steps in the process. Registration and sizing are critical. The size of a contact is frequently two microns or less on one side. The etch depth may approach one micron. Resist definition and adherence over a phosphorus-rich surface is also difficult to maintain. The aspect ratio of resist thickness to opening width can frequently approach one. These factors make resist thickness control and uniformity across the wafer critical factors. Developer cycles must be carefully controlled to avoid both non-uniform development and underdeveloping of small contacts. Adequate wetting of the resist surface and good agitation of the developer are crucial to achieving consistent yield. These are important considerations for resist processing equipment suppliers. Typical CD measurements for this step are shown in Figure 1.1.7-9.

39 CONTACT OXIDE ETCH

Equipment Required: Dry Etch Equipment
Resist Stabilization Equipment
Resist Stripper

This step typically uses a dry plasma etch. Sometimes a combination of plasma and wet chemical etches is used. Critical parameters are selectivity of doped oxide to doped polysilicon, and to resist. This is often difficult with a single dry etch process. Consequently, many fabs use wet etching of the last few hundred angstroms to achieve high uniformity. For device geometries below two microns, dry processing predominates. Dry processing equipment with sequential process capabilities is required if wet etching is not used. Current processes require a slope on the contacts. This can only be obtained with resist erosion techniques using combinations of C_2F_6, CHF_3, and O_2 plasmas. Combinations of bake cycles and resist stabilization techniques are normally required to establish reproducible resist profiles. Resist stabilization systems are also useful for reducing resist burn common to many high etch rate plasma etchers.

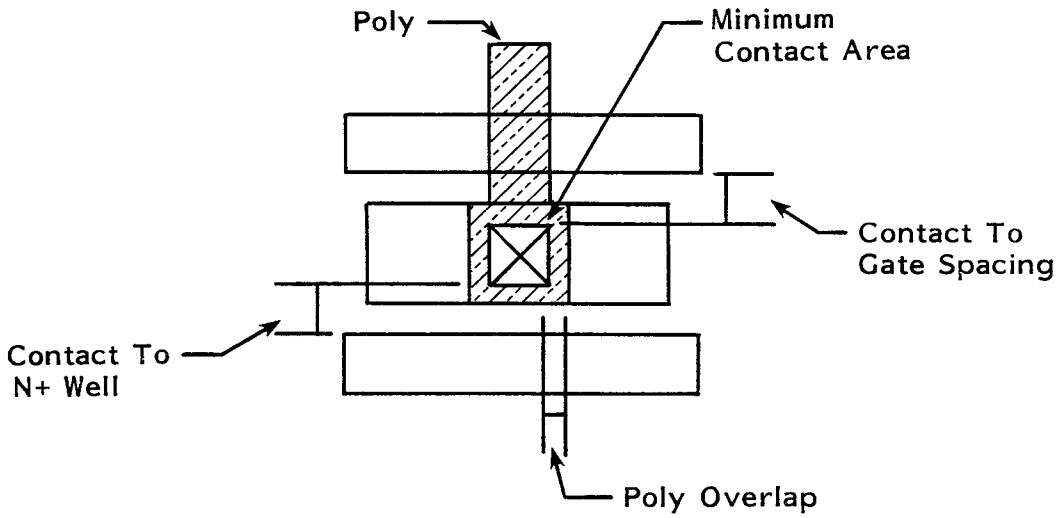
40 REFLOW

Equipment Required: Diffusion Furnace

The vertical slope and ninety degree corners of the contact openings must be carefully rounded to ensure continuity of the subsequent aluminum interconnects. The prior phosphorus gradient through the oxide is one means of control. Other approaches include a controlled erosion of the resist, or the use of a second oversized contact mask. A most common approach is a ther-

Figure 1.1.7-9

Contact Mask Critical Dimensions



TYPICAL MEASUREMENTS
(in microns)

Linewidth	1.0	1.5	2.0
Poly Overlap	0.4	0.6	0.9
Contact To Gate Spacing	0.7	1.1	1.4
Contact To N+ Well	0.7	1.1	1.4
Contact Area	0.9	1.4	1.8

mal reflow to soften the edges of the contact openings. The reflow is achieved by a brief thermal anneal in a diffusion furnace, using a nitrogen or an inert atmosphere. The step has a comparatively low sensitivity to contaminants. Precleans are not used.

41 METAL DEPOSITION

Equipment Required: Sputtering Equipment

AlCuSi films are the most common films in use. They are typically one micron thick. Many control parameters are required to achieve reproducible metal deposition results. Thickness control and uniformity are the two most obvious parameters. Nevertheless, they are also the easiest to control. Less obvious but far more important parameters are grain size, reflectivity, resistivity, and step coverage. Current needs require fourty percent step coverage into 1:1 aspect ratio contacts. Some processes may have contacts which are deeper than their width. This is especially true for the highly planar oxides required for high numerical operature 5X steppers. Bias sputtering is required to increase step coverage. Grain size is controlled by copper content, substrate temperature and deposition rate. A CVD barrier metal may be deposited in the contacts to prevent spiking of the metal into the poly gate. This is also done to plug contacts so that step coverage problems with deep windows is alleviated. Selective CVD tungsten is often required to effectively access very small contacts. Selective deposition is preferred so that additional masking or multiple processing is not needed.

42 METAL MASK

Equipment Required: Steppers
Resist Processing Equipment
Inspection Equipment.

Metal mask is one of the most difficult steps in any high density MOS process. This is primarily due to the dimensional control requirements for the step. Metal mask sizing and registration critical dimensions are comparable to those of gate and contact levels. Design rules usually provide for ‘20% linewidth variation tolerances. Localized losses in linewidth can affect current-handling abilities lead to electromigration failures, as well as limit the amount of metal needed to produce an ohmic contact. Localized line extensions lead to interconnect shorts. Particles on masks or wafers are problematic. Additionally, the rough and irregular surfaces make it difficult to properly expose extremely small dimensions.

The complexity of metallization on today's integrated circuits, coupled with the low defect densities required for reasonable yields, prohibit control by product wafer monitoring. Product lines working with fine feature sizes generally monitor the line itself with test wafers and with particle counters. Multi-level resist processes are used to planarize any contours that affect exposure. This is required when 5X steppers are used. Resist thickness and uniformity is critical as well as alignment, exposure, and develop control. Reproducibility in the develop cycle is usually the key to success at this step. Anti-Reflection Coatings (ARC), dyed resist, Contrast Enhancement Layers, or sputtered coatings are required to limit inteference reflections off the substrate. Automatic alignment is often a severe problem with metal layers. The roughness of metal surfaces must be carefully controlled. Moreover, metal depositions cannot be so planar as to bury alignment marks.

43 METAL ETCH

Equipment Required: Plasma Etcher
Resist Stabilization Equipment
Resist Stripper.

Plasma etch techniques are used exclusively to pattern metal layers on high density processes. Critical parameters are etch rate uniformity and selectivity to resist and doped oxides. Selectivities must be high

enough to allow 50 to 100 percent over-etches without excessive loss of resist or doped oxides. Resist stabilization and bake equipment is essential for good selectivity and resist profile control. Fluorine ion plasma passivation after etch is also essential for corrosion protection. Alloy layers with high copper content may require additional measures for protection against corrosion such as a resist strip prior to removal from vacuum. Special etch conditions are also required to remove copper residues from the wafer. Use of organic strippers is the preferred approach to resist removal. Most inorganic strippers attack aluminum to some degree.

44 ALLOY

Equipment Required: Diffusion Furnace
Rapid Thermal Annealer

A diffusion furnace or rapid thermal annealer is used to sinter and alloy the aluminum-silicon interface. Ohmic contact is obtained at relatively low temperatures, usually less than 450°C. The step is not susceptible to normal contaminants. Precleans are not required.

45 PASSIVATION DEPOSITION

Equipment Required: CVD Equipment

The passivation material is typically a phosphorus doped CVD-deposited oxide that is 12000Å - 15000Å thick. High reliability circuits may employ an additional coating of silicon-nitride or silicon-oxy-nitride for added protection. Preferred deposition equipment includes PECVD and LPCVD systems. The passivation layer should be both stress-free and pinhole free to offer maximum protection for the device's active regions. Hence, gross particles on the wafer, or those accumulated within the equipment, are detrimental.

Wafer precleaning is normally not performed. The wafer usually moves directly from a clean alloy tube to passivation deposition. In the case of inadvertent contamination, wafer cleaning would typically employ an organic resist stripper.

Particles are normally monitored by observing sampled product wafers or lot-included test wafers, under high intensity light with the unaided eye. This oxide is less critical than those requiring dielectric properties.

46-47 PAD MASK & ETCH

Equipment Required:
Aligner
Wet Etcher/Stripper
Resist Stripper

The pad mask level is the least critical with respect to sizing and registration. The major concerns are that the passivation is completely removed from the bonding areas. Residual films on bonding pads can prevent mechanically sound bonds and good electrical contacts.

Advanced Bipolar Processes

A typical bipolar process flow is listed in Table 1.1.7-10. It is a hypothetical two layer metal process with trench type isolation etch. Most leading edge bipolar process steps are covered using this scenario. The following text explains each of these steps.

1 INITIAL OXIDATION

Equipment Required: Diffusion Furnace
Cleaning Equipment

This is the first processing step the bipolar wafer will encounter in the plant. Cleaning considerations are identical to those at CMOS well oxidation. More than half of all product lines omit precleaning. This is a straightforward oxidation with no special requirements for bipolar processes. The only critical parameters are thickness and uniformity control. Film thickness is in the range of 1.0-1.5 microns.

TABLE 1.1.7-10

TYPICAL LEADING EDGE BIPOLAR PROCESS

Step	Process	Equipment Required
1	Initial Oxidation	Diffusion Furnace, Cleaning Equipment
2	Buried Collector Mask	Aligner, Resist Processing Equipment, etc.
3	BC Oxide Etch	Wet/Dry Etch Equip., Rinser/Driers
4	BC Predep	Diffusion Furnace, Implanter
5	BC Drive	Diffusion Furnace, Cleaning Equipment
6	Epi Preclean	Wet Etch, Ultrasonic Scrubbers
7	Epi Deposition	Epi Deposition Equipment
8	Oxidation	Diffusion Furnace, Cleaning Equipment
9	Nitride Deposition	CVD Equipment, Scrubbers, Ultrasonic
10	Isolation Mask	Aligner, Resist Processing Equipment, etc.
11	Nitride Etch	Plasma Etchers/Strippers
12	Silicon Etch	Plasma Etch, Wet Etch Equipment
13	Isolation Predeposition	Diffusion Furnace, Implanter
14	Field Oxidation	Diffusion Furnace, Cleaning Equipment
15	Diffused Base Mask	Aligner, Resist Processing Equipment, etc.
16	Nitride Etch	Plasma Etch/Strip, Wet Etch Equipment
17	Base Predeposition	Diffusion Furnace/High Current Implanter
18	Base Diffusion/Oxidation	Diffusion Furnace, Annealer
19	Resistor Mask	Aligner, Resist Processing Equipment, etc.
20	Resistor Implant	Medium Current Implanter, Annealer
21	Nitride Strip	Plasma or Wet Etch Equipment
22	Nitride Deposition	CVD Equipment, Cleaning Equipment
23	Contact Mask	Steppers, CD Measure Equipment, etc.
24	Contact Nitride Etch	Plasma Etch Equipment
25	N+ Emitter Mask	Aligner, Resist Processing Equipment, etc.
26	N+ Emitter Implant	High Current Implanter
27	Resist Strip	Plasma Stripper, Wet Clean Equipment
28	P+ Mask	Aligner, Resist Processing Equipment, etc.
29	P+ Base Implant	High Current Implanter
30	Implant Activation	Diffusion Furnace
31	Contact Mask	Aligner, Resist Processing Equipment, etc.
32	Contact Etch	Plasma Etch/Strip Equipment
33	Contact Metal Deposition	Sputtering Equipment
34	Sinter/Anneal	Diffusion Furnace
35	Strip	Wet Etch Equipment
36	1st Metal Deposition	Sputtering Equipment, CVD Equipment
37	1st Metal Mask	Aligner, Resist Processing Equipment, etc.
38	1st Metal Etch	Plasma Etch/Strip Equipment
39	Alloy/Anneal	Diffusion Furnace
40	Via Glass Deposition	CVD Equipment, Multiprocess Equipment
41	Planarization Etch	Plasma Etch Equipment, Multiprocess Equipment
42	Via Contact Mask	Aligner, Resist Processing Equipment, etc.
43	Via Oxide Etch	Plasma Etch/Strip Equipment
44	2nd Metal Deposition	Sputtering Equipment
45	2nd Metal Mask and Etch	Aligner, Resist Processing Equipment, etc.
46	Passivation Deposition	CVD Equipment
47	Pad Mask	Contact or Projection Aligner
48	Pad Etch	Wet Etcher

2 BURIED COLLECTOR MASK

Equipment Required: Aligner
Resist Process Equipment

The buried collector represents the first pattern and the first device level to be established in a bipolar process. It is equivalent to a CMOS well mask and etch. The major difference between the two is that in bipolar devices the etched layer is somewhat thicker (typically 2000 Å) and the subsequent collector doping has a higher concentration than does the CMOS well.

This step must be aligned with the best overall locating accuracy and repeatability from wafer to wafer. This is so that subsequent steps will require minimal coarse alignment or operator intervention in automatic alignment. Generally, resist dimensions are not extremely critical. This layer is relatively insensitive to particles and very sensitive to resist pinholes.

3 BURIED COLLECTOR OXIDE ETCH

Equipment Required: Wet/Dry Etch Equipment
Rinser/Driers

Etching of the buried collector layers is normally done with a wet etch process. It uses a buffered, filtered HF etch. Geometries are relatively large, but particulate contaminants can lead to micromasks which leave bits of black silicon on the wafer. Another issue is lack of resist adhesion. This is caused by longer immersion times due to the relatively thick oxide.

Etching and resist strip at this step usually employ wet chemistry, but the use of dry cleaning methods are increasing. Dry etch was initially introduced in support of layers with more critical and more demanding topologies. New lines will likely use plasma at this step, but older, more mature lines will convert at a much slower pace, if at all.

4 BURIED COLLECTOR PREDEPOSITION

Equipment Required: Diffusion Furnace
Implanter

The dopant may be pre-deposited via ion implant, but it is more commonly introduced by a furnace pre-deposition. Epitaxial silicon is to be grown on this surface. Furnace deposition and drive-ins are believed to provide better annealing and silicon surface conditions for epitaxial silicon growth than does ion implanting. Implanting would require dosages on the order of 1E16 ions/cm^2 of arsenic. Substantial silicon damage would result and extensive annealing would be required.

Because of these issues, wafer, furnace, and source purity all become critical purity issues in furnace-based pre-depositions. The temperatures involved, on the order of 900°C, also act to redeposit ionic contaminants. Consequently, additional wafer precleaning is employed regardless of the efficiency of the prior resist strip. An SC1-SC2-HF dip series is typically used, along with intervening rinses and a final rinse and dry.

Antimony trioxide (Sb_2O_3), a solid, is typically used as the dopant source. This material requires additional quartzware in the jungle ahead of the deposition tube proper. The source quartzware is provided with a separate heater to elevate the source temperature so that free antimony can be transported via a carrier gas to the deposition tube.

The source and process gases must be free from metallic contaminants. House-gas receives 0.2 micron filtration at the furnace to minimize particulates that may exist in the lines.

With implantation, the absolute value of dose and uniformity are critical to establish-

ing good threshold control on the finished product. In some exotic processes this step may consist of multiple implants or varying doses and energies. This is done to create special profiles or reduce implant damage. Extremely high energies may be necessary for some applications. Accurate calibration of the ion implanter for correct implant doses and high uniformity is essential to this step.

5 BURIED COLLECTOR DRIVE

Equipment Required: Diffusion Furnace
Wet Cleaning Equipment

This drive-in is of long duration at relatively high temperatures—1 to 2 hours at 1000°C. Hence, ionic contamination is a major concern. Some lines may employ polysilicon, silicon-nitride, or double walled quartz furnace tubes. All gases are filtered at the furnace to 0.2 microns or better.

The wafers will normally have just received a predeposition in the adjacent area. They are off-loaded from predeposition quartz boats onto teflon boats for an interstep oxide dip and then reloaded onto drive-in boats. The purpose of the oxide dip is to remove a highly doped oxide glaze that was acquired in the course of deposition. The reagent is dilute HF—usually 10:1 (H_2O:HF). Dip-offs are often performed in a recirculating filtered bath. The dip is followed by a rinse-dry cycle.

Post process inspection is limited to V/I measurements. Low level ionic contaminants require completion of processing and electrical testing for detection. Unwanted heavy-metal contamination levels may be detected by a residual in-situ test wafer as described in Step 1 on Initial Oxidation. Normally, a blank test wafer will accompany the lot from predeposition through drive-in. This wafer may also be silicon-etched to decorate dislocations.

6 EPITAXIAL PRECLEAN

Equipment Required: Wet Etch
Ultrasonic Scrubbers

This step is perhaps the most critical of all bipolar pre-cleans. An optimum surface is required for the deposited layer of single-crystal silicon so as to atomically bond to the existing silicon and become an extension of that surface. Any contamination of this exposed surface is a major concern. Subsequent operations will re-distribute ionic contaminants throughout the active regions. Particulates are also damaging, in that their presence can cause crystalline deformation and/or act as undesired nucleation sites. Any resulting crystalline damage has the likelihood of further propagation.

Pre-cleans are therefore more elaborate at this step than for most other operations. They also vary by product technologies. Alcohol is commonly used, often with an ultrasonic or brush scrubber, to remove organic residues and particles. Sequential treatment of sulfuric, nitric, and hydrochloric acid formulations interspersed with deionized water rinses are used to remove inorganic contaminants. Finally, the wafer receives a hydrofluoric acid dip, deionized water quench/rinse and filtered nitrogen dry. Ultra-clean chemicals and filtered baths have become the norm for high performance products.

Test wafers are frequently employed at this step to monitor cleanliness. A blank oxidized wafer will first be examined for particulate density, then subjected to the clean, and then reexamined for particulates. It is preferred that no particulates be added in the course of cleaning and further, that the quantity of particles be reduced. Accept/reject criteria will vary with each product line.

7 EPITAXIAL DEPOSITION

Equipment Required:
Epitaxial Deposition Equipment

Epi films are typically one to three microns thick. This step requires ultra clean wafers to ensure good epi deposition with a minimal number of defects. Stacking faults and crystal slip are major considerations at this step. Careful design and fabrication of susceptors is required to reduce these defects. Control of temperature ramp rates is also important in both radiant and RF heated systems. Thickness, resistivity, and autodoping control are other critical parameters. However, they vary in degree of importance depending on the individual process. Control of these critical parameters must be designed into the epi reactor to assure high yield at this point. These critical parameters also pertain to the use of epitaxial films for CMOS devices. General system cleanliness is also important to reduce gross particulate defects. Gaseous HCl is used to clean equipment and wafers in-situ before deposition

8 OXIDATION

Equipment Required: Diffusion Furnace
Cleaning Equipment

The oxide is usually thermally grown and is as thin as practically controllable (250-750 Å±50 Å). Its purpose is to provide stress relief between the subsequent nitride film and the underlying silicon. Because the bare silicon is exposed, cleanliness considerations are the same as at initial oxidation. Inspection is normally limited to verification of oxide thickness and uniformity.

Wafer pre-cleans are normally avoided at this step because the wafer is as clean as it is likely to become following epitaxial deposition. But care must be taken to avoid handling between steps. A corrective clean may be required if a high density of polycystalline spikes are formed in the course of the preceding epitaxial deposition. A typical criteria is 5 spikes for a 100 mm wafer (none ≥ 4 microns high). These protruding defects are hard and brittle. Removal is accomplished manually by applying a razor edge to the spinning wafer while wetted with alcohol. Unfortunately, the removal leaves undesired pits but the step reduces the potential of additional damage by subsequently loosened particles.

9 NITRIDE

Equipment Required: CVD Equipment
Ultrasonic Scrubbers

Nitride deposition for any process is extremely sensitive to particulate contamination. Thickness control of the 500-1000 angstrom film is also critical. This is necessary to avoid color variation in the composite film of nitride and oxide. Color variation can affect exposure and thus dimensional control at the next masking step. Contamination within or under the film is catastrophic and particles on top of the film may have to be removed with scrubbers or ultrasonic cleaners. Gas line particulate control at this step must be addressed in LPCVD equipment. This is done by the utilization of point-of-use filtration and butt-welded, electropolished, 316L stainless steel tubing.

10 ISOLATION MASK

Equipment Required: Aligners
Resist Process Equipment
CD Measure Equipment
etc.

This mask delineates the isolation regions for the active devices. Critical dimensions are more tightly controlled than with the preceding mask. The wafer is sensitive to pinhole-causing-particulates. Subsequent plasma etching of nitride, and silicon in unwanted areas, will also occur in collector regions.

Bipolar VLSI product lines have no less sensitivity than do their MOS counterparts to photolithographic defects. Clean practices in the masking area are based on the most critical mask level involved, as opposed to criticalities of individual mask

levels in process. State-of-the-art bipolar lines use test wafers and particle counters to qualify photolithography lines on a daily basis. The technique is identical to that described for MOS in Step 2, as are the clean maintenance practices.

11 NITRIDE ETCH

Equipment Required: Plasma Etchers
Strippers

This etch is performed with dry plasma in the more advanced product lines. Barrel plasma etching, using a binary mixture of oxygen and tetrafluoromethane (CF_4), is one approach. Barrel etching requires a subsequent etching of the underlying oxide. It is usually a wet etch. Planar plasma etching with CF_4 plus 8% oxygen will remove silicon nitride and silicon oxide layers in one step. Both require cleanliness prior to etch, the latter being more sensitive as a result of the anistropy of the all-dry planar etch. Particle foot prints will be reproduced, blocking the isolation deposition in localized areas. The contamination considerations of plasma etching were discussed in more detail in Step 9 of the MOS process.

This process step requires a post etch resist strip.

12 SILICON ETCH

Equipment Required: Plasma Etch
Wet Etch Equipment

The purpose of this etch is to physically remove silicon from the surface so as to create a moat around the active transistor. This region will later be doped and oxidized. The regrown oxide will provide dielectric isolation in addition to underlying diffused isolation for circuit transistors.

The etch may be performed by either wet or dry methods, the latter being preferred for fine-geometry product lines. The main critical parameters are undercutting and wall profile. Secondary parameters are etch rate, selectivity, and uniformity. SiF is the preferred gas for this application. Etch system cleanliness is important from the standpoint of post-operation residual particulates. Particulates will interfere with the subsequent predeposition. Isolation leakage currents may result.

13 ISOLATION PREDEPOSITION

Equipment Required: Diffusion Furnace
Implanter
Wet Cleaning Equipment

The exposed isolation areas are doped by either diffusion furnace or ion-implant methods. The use of a furnace implies the exposure of substrate silicon, at temperature. While isolation rings do not play an extremely critical part in device performance, a pre-clean is employed. It is usually limited to a brief 10:1 HF dip. This may be preceded by SC1 or SC1 and SC2 cleans depending on the cleanliness of line handling and storage.

Modern lines mostly use an ion implanter to provide a relatively high dose of boron, 1E15 ions/sq. cm. Implants will vary greatly depending on the individual process and whether an actual diffused isolation is required or merely a channel stop. Generally this step is non-critical. However implant angle may be a consideration in some trench implants. Precleans are normally not used due to the low temperatures involved. A nitride is used as the implant mask, rather than a resist, so chemical cleaning can be performed if necessary. Sulfuric-peroxide is the usual choice, if used.

14 FIELD OXIDATION

Equipment Required: Diffusion Furnace
HIPOX Equipment
Cleaning Equipment

The doped isolation areas are next oxidized in an oxidation furnace. Oxides are grown only in these exposed areas, the balance of the wafer surface being shielded by the remaining nitride. The temperatures must be kept low, less than 950°C, to prevent liberation of nitrogen from the nitride and

the buildup of sidewall stresses. Atmospheric oxidation at this temperature requires nearly 20 hours to provide the 1 to 2 micron oxide required. Consequently, many product lines use high pressure oxidation (HIPOX).

In any event, the lower temperatures do limit the migration of contaminant ions. Notwithstanding, wet precleans are employed. Cleans are designed to remove the particulates acquired in handling and handling mechanisms in the preceding ion implantation and subsequent transport, as well as ionic contaminants that can lead to isolation leakage currents.

Field oxidations are usually non-critical operations. They have moderately broad thickness and uniformity specifications. However, newer trench processes put stringent requirements on this step as overall thicknesses are scaled down. The overall thickness becomes a consideration for trench filling to ensure closure of the trench without excessive stress. Trench isolation techniques are seeing increased usage in Bipolar VLSI processes.

15 DIFFUSED BASE MASK

Equipment Required: Aligner
Resist Process Equipment

For most bipolar processes this step is usually an oversize mask to expose regions which require a low resistance base diffusion. Cleanliness and freedom from pinholes are crucial and dimensional tolerances may be a factor if the mask establishes the lengths of resistors. For those applications, use of 5X steppers will predominate because of its greater resolution capabilities compared to scanning aligners. The requirements of cleanliness and freedom from pinholes will effect customer specifications regarding purchases of resist processing equipment.

16 NITRIDE ETCH

Equipment Required: Plasma Etch
Wet Etch Equipment
Stripper

The etch considerations here are similar to those described in Step 11 but are more critical. Cleanliness prior to etch is mandatory. Step 11 involved an isolation region which prevents device interaction. Here, the base is a part of the active device proper.

Base nitride etching can be performed via wet chemistry or by dry plasma techniques. A two step, dry or wet nitride etching followed by wet oxide etching, has the advantage of selectivity; i.e., the underlying silicon is not etched. An all-dry method requires good end point detection to prevent attacking the underlying silicon. Recirculating filtered etching baths are common at this step when wet chemistry is employed. Photoresist removal is required after etch.

17 BASE PREDEPOSITION

Equipment Required: Diffusion Furnace
Wet Cleaning Equipment
High Current Implanter

Base predeposition may be performed by either ion implant or furnace tube methods. There are some critical depth parameters and less critical V/I parameters. A high current implanter is used for this step when V/I is a major consideration, as with newer bipolar devices. The preceding etch and resist strip must be thorough and the implanter end station clean of particulates to avoid implant blocking.

Furnace tube methods employ wet precleans due to the temperatures involved. Here, critical lines would employ an SC1-SC2-HF dip. Furnace operations also employ a 10:1 HF wafer deglaze after depositions. The tube itself requires periodic

removal and wet cleaning to remove doped quartz as well as quartz and silicon particulate debris. While variable, this type of clean (described in Step 1 of the MOS Process) takes place every 3 months, on average. Furnace operations require 0.2 micron filtration of house gases.

18 BASE DIFFUSION/OXIDATION

Equipment Required: Diffusion Furnace

The diffusion following base predep must be controlled for both time and temperature. This is necessary to ensure a reproducible junction depth and sheet resistance. Diffusion furnaces are typically used for this process. Films are typically 0.5-1 micron thick.

19 RESISTOR MASK

Equipment Required: Aligner
Resist Process Equipment

This step is usually an oversize mask to block an implant. Cleanliness and freedom from pinholes are crucial to avoid blocked implants or unwanted implanted areas. This is a non-critical process and scanning aligners are satisfactory. Important trends affecting process equipment at this step are particulate-free dispensing of photoresist.

20 RESISTOR IMPLANT

Equipment Required: Medium Current Implanter
Annealling Equipment

Resistor implants vary over a broad range of energies depending on the process. They are frequently B+ in a dose range of 1E13 to 1E15 ions/cm^2. This causes a partial disruption of the crystal lattice which is difficult to anneal without excessively high thermal processing. Consequently, the lattice damage issue has tended to drive energy levels down. Lower energy levels make the damaged layer thin enough to be consumed by the subsequent oxidations. The use of rapid thermal annealers will proliferate in order to substantially reduce thermal budgets so that higher energy levels can be used.

21 NITRIDE STRIP

Equipment Required: Dry or Wet Etch Equipment

This step involves the removal of the balance of nitride originally deposited in Step 9. Stripping may be accomplished by wet or dry methods. Barrel plasma etching is common. Nitride films contain oxynitride ($Si_xO_yN_z$) and nitride hydrides ($Si_xH_yN_z$) in addition to silicon nitride. Fluorine based plasmas are effective in removing all these species. Selectivity is not an issue where underlying strata is wholly field oxide. Product lines using wet chemistry employ hot phosphoric acid as an etchant. It is important than the surface be stripped clean without residue to ensure the uniformity of the following deposition.

22 NITRIDE DEPOSITION

Equipment Required: CVD Equipment
Wet Cleaning Equipment

Nitride is once again deposited, typically via plasma enhanced chemical vapor deposition (PECVD). The prior nitride Step (#9), was deposited immediately after a clean oxidation step. Here, the wafer has had additional exposure to contaminants. Some lines employ a wafer preclean for particulate removal. Sulfuric-peroxide is used for organic particulates. High pressure on brush scrubbing may be employed. The nitride layer must be uniform to insure complete etching of windows, where required, and a pinhole free strata elsewhere.

Process gases employ point-of-use filtration to minimize piping particulates, and are required to be free of oxygen and moisture.

23 CONTACT MASK

Equipment Required: Aligner
CD Measure Equipment
etc.

This step defines contact areas in the nitride layer. It also sets the size of the emit-

ter areas in at least one dimension. The CD control required for this mask usually makes it a critical mask layer. Consequently, steppers predominate for linewidths and resolution requirements below two microns. Cleanliness and freedom from pinholes are crucial to avoid shorts between adjacent regions when the contact metallization is done.

24 CONTACT NITRIDE ETCH

Equipment Required: Plasma Etch Equipment

Planar plasma etching is the preferred method for smaller geometries. Fluorine based plasmas are used. Common sources are CF_6 or CF_4 in a binary mixture of oxygen. This etch technique is anistropic. Particulates residing in areas to be etched may block or limit the etch in localized areas. Maintenance of a clean reactor chamber is therefore important. Isopropyl alcohol wipedowns, several times a shift, are the rule for critical product lines.

25 N+ EMITTER MASK

Equipment Required: Aligner
Resist Processing Equipment
etc.

This mask is an oversized blocking mask. Only emitter regions and base contact regions will be 'opened-up' for the following high dose emitter implant. Resists may receive deep UV or photomagnetic curing to stabilize the polymer, affording greater tolerance to this dosage. Particulates in opened areas can be detrimental in that they can block or deflect the ion beam in localized areas.

26 N+ EMITTER IMPLANT

Equipment Required: High Current Implanter

This high dose (1E15-1E16 ions/cm^2) arsenic implant is achieved by one of several high current implants. High currents predicate wafer cooling. Dose and energy control are critical to electrical parameters. Wafer handling and chambers must not add particulates, for the reasons cited in Step 25.

27 RESIST STRIP

Equipment Required: Plasma Stripper
Wet Clean Equipment

Removal of resist after hi-current implants and/or deep UV bake is more difficult than it is in other steps. The high currents involved create complex polymer linkages. Stripping is typically a two step process. The first step is bulk removal via plasma oxygen ashing. This is followed by a hot-sulfuric/peroxide acid treatment to remove remaining residues, which is then followed by a de-ionized wafer rinse and dry. Residues have been reported to contain dopant arsenic. Complete removal is required to eliminate potentially unwanted dopant sources as well as particles. Advanced lines question the adequacy of this process, even after repeated sulfuric-peroxide treatment. Several vendors have offered non-phenolic organic strippers with purported improved removal efficiency. There is no strong evidence from industry users that this problem has been solved.

28 P+ MASK

Equipment Required: Aligner
Resist Stabilization Equipment
etc.

This mask is normally an oversize blocking mask used to shield n regions from the p+ implant. The main criteria at this step is to ensure that the resist will tolerate the high dose implant it will be exposed to. Deep UV resist stabilization or photomagnetic curing of the resist is necessary to minimize damage problems during the implant.

29 P+ BASE IMPLANT

Equipment Required: High Current Implanter

This is a high dose implant (1E14-1E16) of low energy boron. The implantation is

followed by a resist strip. Considerations cited in Steps 26 and 27 are applicable.

30 IMPLANT ACTIVATION

Equipment Required: Resist Strip
Diffusion Furnace
Rapid Thermal Processor

After resist strip implanted wafers will require an implant activation step and possibly an oxidation step. All dopants have by now been implanted in the remaining active regions. Activation of the implants is required. It must be controlled accurately for both time and temperature to ensure reproducible results. It may be performed by a rapid thermal annealer or within a diffusion tube. This is the last high temperature operation (approximately 900°C) the wafer will see, other than at alloy. Surfaces are, however, protected by oxide from contaminants so precleans are normally not employed. If only activation is required then rapid thermal processors are useful. If oxidation is required then diffusion furnaces are preferable.

31 and 32: CONTACT MASK & ETCH

Equipment Required:
Steppers, Inspection Equipment
Resist Processing Equipment
Plasma Etch/Strip Equipment

Bipolar processes are identical to MOS processes. See Steps 38 and 39 of the prior MOS process.

33 CONTACT METAL DEPOSITION

Equipment Required: Sputtering Equipment

Shallow junction devices require the deposition of a noble metal in the contact areas and the formation of that metal's silicide at the surface. This limits the depth of sintering that can occur with subsequent interconnect metals. Deposition thickness control is exercised to ensure sufficient silicide formation and prevention of emitter base shorts by the Schottky diode. Good oxide removal in the contact areas prior to deposition is necessary to insure good ohmic contact.

The material used is typically platinum, deposited by sputtering techniques, using ionized argon. The gas must meet very stringent cleanliness and purity requirements. The presence of contaminants alters the film composition and seriously affects the sputtering process. Moisture, oxygen and hydrocarbons are to be avoided.

Systems that provide bias-sputter etching are particularly useful because any residual oxides in the contact areas may be removed by back bias sputter-etching techniques. However, sputtering equipment, H also deposits material on other surfaces as well as onto the wafer. This material can build up to the point where particles may be abraded or loosened from the surface and then be redeposited onto the wafer. The target itself may slough off unwanted materials. Periodic removal of this material and cleaning of the chamber and internal hardware is required.

Equipment design should be such that targets are not located above the wafer and that pump down and vent cycles do not create turbulence. Turbulence can redeposit particulates that may have formed on chamber walls.

34 SINTER/ANNEAL

Equipment Required: Diffusion Furnace

This operation sinters the deposited metal in contact with the underlying silicon, forming the desired silicide. The operation generally takes place in a diffusion tube at 350° - 400°C with a forming gas atmosphere. The operation is not regarded as particularly sensitive to contamination. Wafer cleans are not required.

35 STRIP

Equipment Required: Wet Etch Equipment

The remaining metal not converted to silicide is removed by wet etching. Aqua regia or hydrochloric (HCl) and nitric acid (HNO_3), 3:1, is the etchant, followed by deionized wafer rinsing and drying. A thorough rinse and dry with filtered D.I. wafer and nitrogen is required. Subsequent particulate contamination in the contact areas will interfere with good ohmic contact of subsequent metals.

36 1ST METAL DEPOSITION

Equipment Required: Sputtering, CVD Equipment

On shallow-junction bipolar lines, a barrier metal will be deposited prior to aluminum deposition. This will prevent the migration of aluminum into the silicon and the consequent hazard of shorted junctions. Barrier metals are typically either tungsten or titanium-tungsten with a typical thickness of 0.2 microns. Barrier metal composition must be well controlled with respect to composition and contamination. It must be pinhole-free to perform the required function. Deposition techniques may use either sputtering or chemical vapor deposition. Sputtering is more typical.

Aluminum-Copper-Silicon is deposited directly on the preceding material. The thickness of typically 0.5 micron is required for uniformity. Materials composition uniformity, and hence etch uniformity, are best controlled with sputtering deposition techniques.

Care must be exercised in handling or storage between the barrier metal and the aluminum depositions. Particles accumulated on the surface will be trapped between the metal layers and prevent lamination in localized areas. For this reason, multiple-target sputtering systems are preferred, so that both metal systems can be sequentially deposited. Equipment cleanliness and gas purity are required, as discussed in Step 32. Wafer precleans are not normally employed.

37 1ST METAL MASK

Equipment Required: Aligners
Resist Processing Equipment

Metal mask is one of the most difficult steps in any high density process. This is primarily due to the dimensional control requirements for the step and the difficulty in properly exposing extremely small dimensions on a rough and very irregular surface. Resist thickness and uniformity is critical as well as alignment, exposure, and develop control. Reproducibility in the develop cycle is usually the key to success at this step if steppers are used for pattern exposure. Processes using projection aligners must also have good control over all aligner parameters which effect image contrast. Anti-reflection coatings may be required to achieve adequate resolution and automatic alignment may be a severe problem if the metal layer surface roughness is not carefully controlled.

38 1ST METAL ETCH

Equipment Required: Dry Etch/Strip Equipment

Dry etch techniques are used to pattern metal layers on high density processes. Critical parameters are etch rate uniformity and selectivity to resist and to develop underlying materials. Selectivities must be high enough to allow 50 to 100 percent overetches without excessive loss of resist or poly exposed when the metal layer is removed. Resist stabilization and bake equipment is essential for good selectivity and resist profile control. Fluorine ion plasma passivation after etch is also essential for corrosion protection. High copper alloy layers may require additional measures for protection against corrosion, such as a resist strip prior to removal from the vacuum. Special etch conditions are also required to remove copper residues from the wafer.

39 ALLOY/ANNEAL

Equipment Required: Diffusion Furnace

This step is usually considered a non-critical furnace step. Temperatures are on the order of 450°C in a hydrogen nitrogen atmosphere. Temperature is somewhat critical. Newer processes which make use of oxygen donor effects require more careful consideration of temperatures.

40 VIA GLASS DEPOSITION

Equipment Required: CVD
Multiprocess Equipment

Steps 40 and 41 may be combined into one continuous process with multiprocess equipment. The purpose of this step is to provide a dielectric between the 1st metal and subsequent 2nd metal interconnects. A PSG/BPSG glass is deposited. It is relatively thick, 1.0 micron, and doped by phosphorus and, occasionally, by boron. Dopant uniformity control is required. The layer must be free of occluded particles, particularly when a subsequent planarization etch is to be employed (See Step 41, following).

The incoming wafer should be free of particulates, implying a good resist strip at the prior metal mask and careful interim handling. Cleaning is normally avoided because the metal traces are exposed. Notwithstanding, inadvertent contamination may be reduced by an organic resist strip treatment.

The deposition equipment is carefully monitored by UV inspection of product and/or test wafers for particulates. Particle counters may be employed. Periodically scheduled quartz cleaning is performed. Wet cleaning may be as frequent as every 15 to 20 runs, depending on the equipment used and product sensitivities.

41 PLANARIZATION ETCH

Equipment Required: Plasma Etch Equipment
Resist Processing Equipment
Multiprocess Equipment

Two Methods are commonly used. One is the sacrificial resist method. The other involves using a multiprocess system with an isotrophic etch. This step is a relatively new and unique application of plasma etching. The sacrificial resist method requires that the wafer is coated with resist, exposed without patterning and cured. Resist is normally thinner over steps (corners) and thicker on planar surfaces away from corners. The resultant surface now has 'smoothed' edges. The wafer is next etched in plasma with a highly non-selective gas, e.g., equivalent etch rates for the photoresist and the underlying doped oxide. Exposure to the reagent for sufficient time will result in complete removal of resist and a portion of the underlying oxide. The resultant surface will have the same profile.

The multiprocess system method incorporated both steps 40 and 41. It eliminates the need for resist deposition. However, surfaces are not as planar as with the sacrificial resist method.

42 VIA CONTACT MASK

Equipment Required:
Aligners, Resist Process Equipment
Steppers, CD Measure Equipment, etc.

This step is particularly challenging to photolithography. Via contacts are small, down to two to four times the wave length of the light being used for exposing the resist. The aspect ratio of resist thickness-to-opening width can approach 1:1. Despite the previous "planarization" etch, the surface is not planar (edges are smoothed). The underlying oxide is also phosphorus doped, detract

ing from resist adhesion. The situation is nearly identical to the MOS case in Steps 38 and 33 of that process and is treated in the same manner.

43 VIA OXIDE ETCH

Equipment Required: Dry Etch Equipment

This step can be either completely dry etch or be a combination of dry and wet chemical etches. Wet etching of the final few hundred angstroms assures high selectivity. However, as device geometries decrease, wet etching will no longer be applicable. Therefore, dry processing equipment with sequential process capabilities will predominate. Critical parameters are selectivity of the etch to doped poly, doped silicon, and resist. *Etch* uniformity is important. It cannot be traded off for *etch rate* uniformity because varying film thicknesses on different parts of the same die dictate large overetches. Current processes also require some degree of slope on the contacts which can only be obtained with resist erosion techniques using a C_2F_6, CHF_3, and O_2 plasma. Combinations of bake cycles and resist stabilization techniques to establish reproducible resist profiles are normally required with very small contacts. Resist stabilization systems will also see increased use for reducing the resist burn phenomena common to many high rate plasma etchers.

44 2ND METAL DEPOSITION

Equipment Required: Sputtering Equipment

Many control parameters are required to achieve reproducible metal deposition results. Thickness control (0.8 microns of AlCuSi) and uniformity are the two most obvious parameters. However, these are also the easiest to control. Less obvious but equally important parameters are grain size control, reflectivity control, and resistivity control as well as good step coverage. Use of deposition systems with bias sputtering capabilities will grow in order to effectively cover steps. Alloy composition control is also critical if reproducible etch results are to be obtained. For second layer metal processes a sputter clean must also be done prior to metal deposition to remove any residual via glass and aluminum oxide from the contact openings. Sputtering systems incorporating reverse-bias back sputtering or ion milling are increasingly used for this process.

45 2ND METAL MASK AND ETCH

Equipment Required:
Steppers, Resist Stabilization Equipment, etc.

This process is identical to 1st Metal Mask and Etch.

46 PASSIVATION DEPOSITION

Equipment Required: PECVD
APCVD

This layer must be low stress and pinhole free. Oxides must be carefully controlled in dopant concentration if corrosion problems and cracking problems are to be avoided. PECVD Nitride or oxynitride must be tightly controlled for composition and stress to avoid cracking and delamination problems.

47-48 PAD MASK AND ETCH

Equipment Required: Aligner or Projection Aligner

These steps are identical to steps 46 and 47 for MOS technology.

1.1.8 Technological Driving Forces

In contrast to other industries, planning organizations in semiconductor manufacturing must be much more attuned to technological change. This is because a new semiconductor manufacturing plant can grow obsolescent in just two years time. It will usually be obsolete by it's fifth birthday. Companies must constantly renovate and rebuild manufacturing capacity. For example, NEC completely rebuilds all of its semiconductor manufacturing capacity every five years. This technological pace plays a critical role in determining the success or failure of both semiconductor companies and equipment suppliers. The role that technology plays is felt in three key ways:

The current state of semiconductor technology determines the relative size of an equipment market; evolutionary technical development determines market growth; and revolutionary technical upheaval determines major shifts in equipment demand. In practice, all three are in a constant state of flux. Consequently, their effects must be well understood to be successful in the semiconductor manufacturing industry.

The pace of technological change is not the only factor that is important in semiconductor manufacturing. As was shown in Section 1.1.6.2, mere extrapolations of trend lines can be quite misleading. Consequently, it is also important to understand the forces that drive change in semiconductor manufacturing.

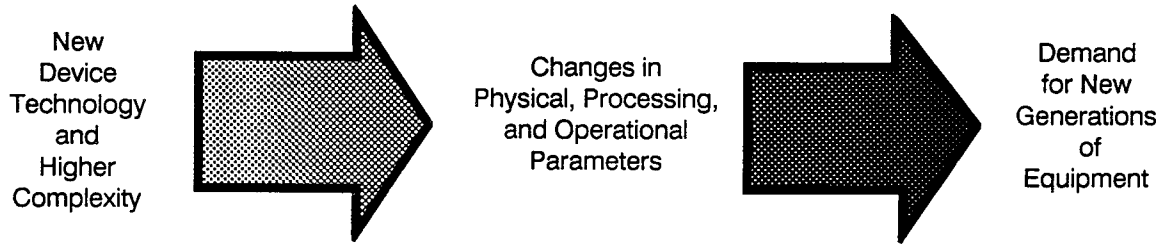


Figure 1.1.8.0-1

Forces Driving Change in Semiconductor Manufacturing Equipment

Technological driving forces start with a demand for new device technology and higher complexity (see Figure 1.1.8.0-1). These two forces will drive changes in the physical, processing and operational parameters of the device. Change in these factors will inturn, change the way in which devices are manufactured. New manufacturing requirements drive demand for new generations of equipment.

This section examines how both technological pace and its characteristics drive change in semiconductor manufacturing. Section 1.1.8.1 focuses on technological pace. It shows how technological pace can be used to determine equipment demand. Section 1.1.8.2 focuses on the characteristics of manufacturing technology. It shows how the various facets of semiconductor technology affect manufacturing and equipment.

1.1.8.1 Techlogical Pace

This section shows how to derive equipment demand from the various technical forces that drive manufacturing. Conversely, the same approaches can be used to show how equipment either limits or expands the ability of the semiconductor industry to grow. For the purposes at hand: Technological pace has been segmented into three basic types. Technology's current state, evolutionary development, and revolutionary development. How each affects the market is examined below.

The current state of technology is the easiest to explain since it is the basis for an equipment market's size. There is almost a pure mathematical relationship that exists between the current state of technology and the size of any given equipment market. This relationship is founded on the basic premise that a company must produce a product before it can be sold. In turn, a company must have the capacity to produce the product.

The most basic measure of production in a wafer fabrication plant is the wafers itself. Packages, or die, are the key measure of production in test and assembly. Total demand for equipment can be determined by tracking these measures of production. The following example illustrates how the two interrelate so as to determine market size for high current ion implanters:

> There were 135 million wafers processed in 1984. Over 95% of these were for integrated circuit production. There are essentially two process technologies used for semiconductor manufacture: Bipolar and MOS. MOS accounted for 57.9 million wafer starts in 1984. Bipolar accounted for 68.1 million wafer starts.
>
> All MOS processes use ion implantation. There are typically two high current steps per MOS wafer. Ion implanters average a throughput of 50 wafers per hour. This throughput allows an implanter to process roughly 0.25 million wafers per year. Consequently, 57.9 million wafers times two steps divided by a 0.25 millin wafer throughput yields a total demand for 463 high current ion implanters in 1984. In 1983, 38.3 million MOS wafers were started. Consequently, 306 high current ion implanters were needed to produce 1983's MOS integrated circuit sales. The difference between 1984's 463 high current ion implanters and 1983's figure of 306 systems is the amount of new machines needed to sustain semiconductor growth. This would equate to a demand for 157 new high current ion implanters. This amounts to a sales potential of $188.4M at an average selling price of $1.2M each. This figure is reasonably close to the $198.2M in sales that actually were recorded in 1984.

Market demand for virtually any type of equipment can be determined by the equation used in the ion implanter example. This equation is shown below:

$$D = \frac{\Delta P \cdot S}{U} + R \qquad (1)$$

Where:

D = Market demand in units.
ΔP = Year to year change in production volume in units.
S = Number of steps per unit of production.
U = Annual system throughput in units.
R = Replacement

The equation is a static state calculation of demand for one year. The way in which both evolutionary and revolutionary technical change affect the market can also be derived from this equation by adding a time element.

Market growth is determined by two factors, one is market driven and the other is technically driven. Routine market growth in production drives an increase in P, the year to year change in production volume. Technological change drives a multiplicative increase in S, the number of steps per unit of production. Thus, it can be seen that technological change can have a more powerful effect on market demand than routine

market growth. For example, one new implant step added to manufacturing increases the effective market size by 50 percent. Whereas, wafer starts would have to grow by 50 percent to drive the same growth level through market expansion.

Evolutionary Technical Change

Evolutionary technical change has a major impact on accelerating market growth for semiconductor equipment. Evolutionary change can be characterized as those developments which result from continued improvement of an existing technology. They tend to be time dependent and are reasonably predictable. For example, Moore's law is one example of evolutionary technical change. It states that memory size for ICs doubles each year. This law has held for the better part of two decades. Even today, device complexity continues to advance a rate of 1.5 times per year. Steady improvements in linewidth resolution, ion implantation, plasma etching, etc. have made these advances possible. The result has been a steady predictable growth in processing complexity as shown in Figure 1.1.8.1-1.

These factors are reasonably easy to quantify into equation 1. When time and technological changeover are accounted for, each variable has a different value for any given period (for example, a quarter or a year). Equation 1 will thus be quantized in the following manner:

$$D_{\tau+\eta} = \frac{\Delta P_{\tau+\eta} \cdot S \cdot (1+T)}{U_{\tau+\eta}} + R_{\tau+\eta}$$

Where:

- τ = Base period for a projection. The end of the current period. Unless otherwise stated it is assumed that is the base year from which a projection begins.
- η = Time represents the number of periods forward in time that is being projected.
- T = Evolutionary Technological change factor. This is measured by the compound annual growth of steps per unit of production.

This equation can also be used to show how and what percent of the equipment industry's growth is due to evolutionary technical changeover and what percent is due to capacity requirements.

The growth in process complexity has been well documented as being a key factor driving growth in equipment sales. As was mentioned previously, each additional step has an multiplicative effect on equipment demand. The technological growth factor between 4K bit Dynamic RAM's and 4 Megabit DRAM's was about ten times. The peak production year for 4K Dynamic RAM's was around 1977. The peak production year for 4 Megabit DRAM's is expected to be around 1990. Consequently, the compound growth in technical complexity has

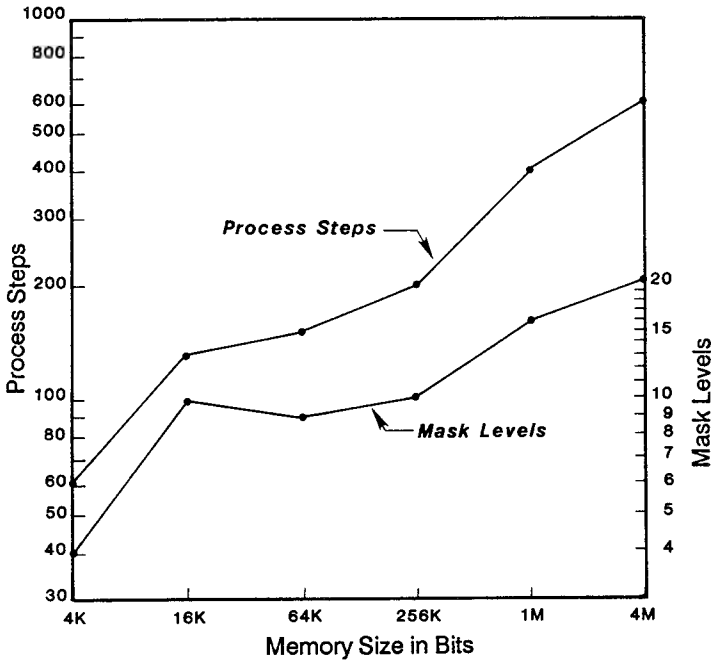


Figure 1.1.8.1-1

EVOLUTION OF PROCESS COMPLEXITY
(DRAMS)

been 19% per year. The semiconductor equipment market will average a 23% compound annual growth over this same period. Thus, roughly 83% of all semiconductor equipment growth is technologically driven, while only 17% of its growth is capacity driven. This is shown below:

SEMICONDUCTOR MANUFACTURING EQUIPMENT GROWTH SOURCES

Driving Force	1977-1990 CAGR	Percent of Overall Growth
Technological Change	19%	83%
Capacity Expansion	4%	17%
Overall Growth	23%	100%

110-T5

Consequently, evolutionary technical change is the primary driving force of growth in equipment sales.

Revolutionary Technical Change

Revolutionary technical change in manufacturing determines major shifts in demand from one type of equipment to another. It can be characterized by those developments which result from technical breakthroughs. The nature of these breakthroughs are highly unpredictable and cannot be forecasted. They usually occur at times when the evolution of existing technology fails to progress. Typically, it runs into a key technical limitation that cannot be overcome. Consequently, a new and radically different technology emerges to take the place of the older technology.

The shift from projection aligners to wafer steppers in the early eighties is a primary example of revolutionary technical change-over. Projection aligners went through four evolutionary generations in the mid-to- late-seventies. They were the dominant lithography tool in use at the time. Four to five micron resolution was routinely achievable by the mid-seventies. Submicron resolution was available in 1981 with the advent of DUV projection. However, overlay registration emerged as a new technical problem when the industry passed below two micron geometries. The first generation of DUV projection aligners was not capable of achieving the required registration. The advent of the wafer stepper solved the registration problem thereby allowing the industry to progress. This single technical limitation paved the way for the wafer stepper. The impact on market share was dramatic. The lithography market share held by wafer steppers rose from 7% in 1978 to 56% in 1984. Projection aligners share of the market fell from 61% in 1978 to 28% in 1984. Today the shares stand at 70% and 15%, respectively.

However, this revolutionary change had little measurable impact on the market growth for wafer exposure equipment. The total wafer exposure equipment market grew from $46.3 in 1975 to a 1980 peak year of $269.5M–a compound annual growth rate of 42%. The compound annual growth between 1975 and the peak year of 1984 was 40%. The reason for this lack of additional market growth is that while steppers cost twice as much at one-half the thruput of a projection aligner, they achieved much higher yield. Consequently, the net cost per good die was actually lower. Thus, the change in overall market potential was not measurable. This is not to say that revolutionary technological change does not contribute to market growth. The semiconductor market would have stagnated without the advent of the wafer stepper. Revolutionary technological change allows for the steady progression of market demand. It causes major competitive shifts within markets. However, it seldom accelerates growth in equipment sales.

1.1.8.2 Characteristics of Technological Driving Forces

The ways in which technological change can occur is multifaceted. Figure 1.1.8.2-1

shows the various technology driving partitioned into four major paths for equipment development. These paths are labeled: Device technology, device complexity, processing parameters, and operational parameters. Each of these have several important subsegments that are important drivers of equipment developments.

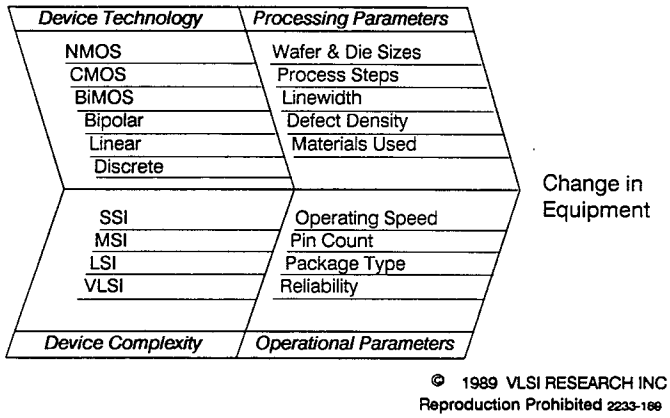


Figure 1.1.8.2-1

Technology Driving Forces

It can be seen that these four major categories quickly multiply into 480 sub-categories. These will again unfold into numerous rivulets of specialization. The possible combinations and permutations is virtually infinite. Consequently, it is necessary to limit the scope of any analysis to be able to comprehend the significant forces that drive technology. In the work that follows, technological driving forces will mainly be discussed according to how they pertain to processing parameters and operational parameters. These are generally the ones which will more directly affect manufacturing equipment. Device technology and complexity tend to serve as drivers of processing and operational parameters. Consequently, device technology and complexity will be largely ignored except as it relates to these parameters.

PROCESSING PARAMETERS

Processing parameters make most of their impact felt on wafer fabrication equipment. Changes in these parameters largely determine a need for new manufacturing equipment generations. They also provide a measure of the manufacturing prowess of a semiconductor company. Consequently, they are important business drivers for semiconductor manufacturers. There are five key parameters that are the most critical. They are:

- wafer and die sizes
- process steps
- linewidth
- defect density
- materials used

Wafers are the one common denominator throughout the semiconductor industry. They provide a readily available yardstick against which both manufacturers and the industry can be evaluated. The revenues that a semiconductor manufacturer can generate from a square inch of silicon is an excellent measure of its marketing prowess. It's manufacturing prowess can be measured by its cost to produce that same square inch of silicon. These costs are largely controlled by wafer size and die size. Wafer sizes are continually increasing. So too are die sizes. Just how large they have been growing can be placed in somewhat better perspective by Figure 1.1.8.2-2. Wafer size changes has been one of the most important driving forces of change in wafer fabrication equipment.

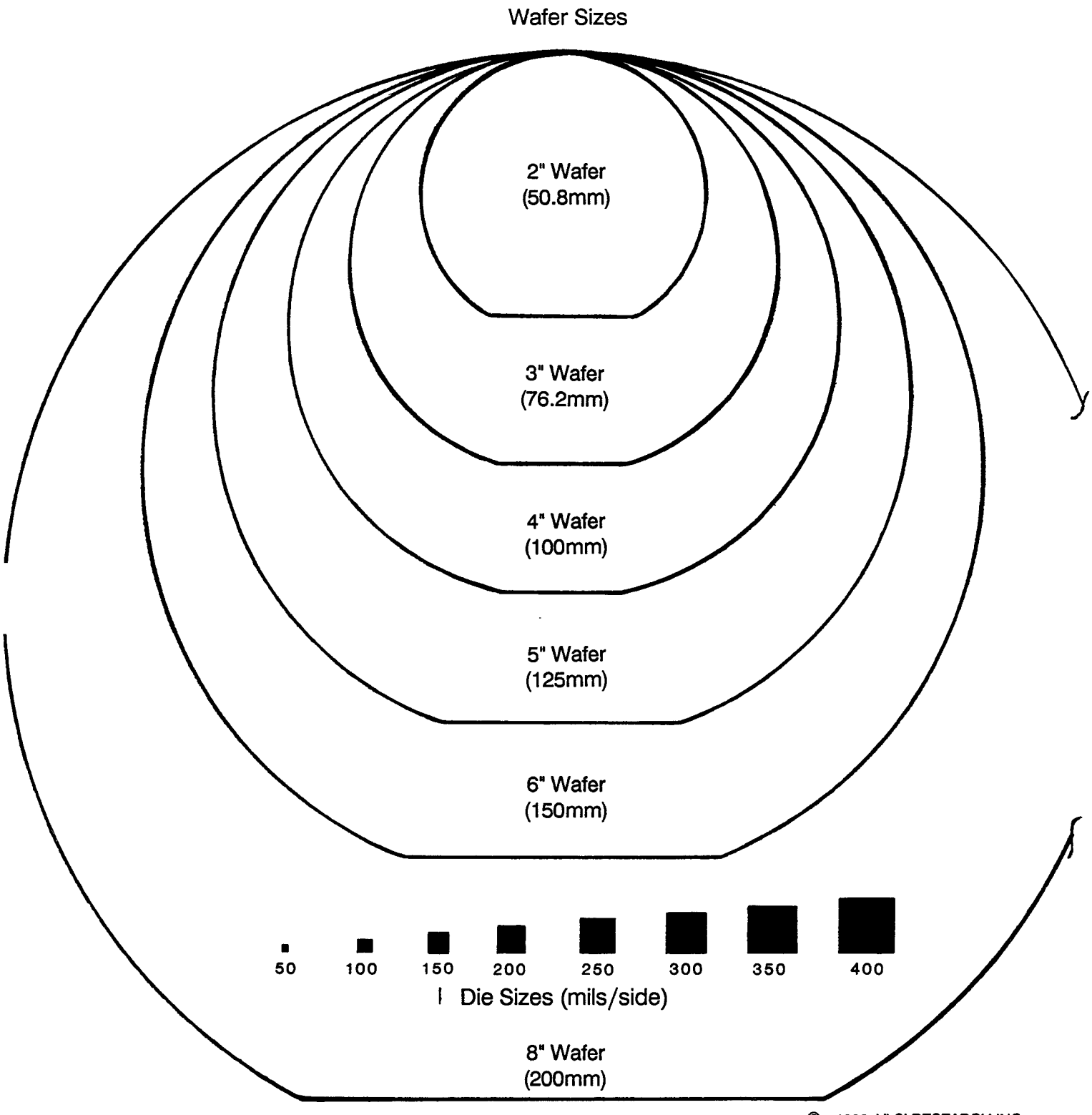


Figure 1.1.8.2-2

VARIOUS WAFER & DIE SIZES

Equipment manufacturers will invariably place wafer size parameters high on their list of trends to watch. Seemingly minor changes in wafer size—either diameter or thickness—can wreak major design changes in new equipment. It immediately obsoletes older equipment, thereby creating new demand. Consequently, from an equipment manufacturers viewpoint, accurate prognosis of wafer size changes is of prime importance.

Die sizes are an important parameter because of their relevance to device complexity, yield, and manufacturing economies. The most simplistic of these relationships is how die size and wafer size interrelate. Each die is an integrated circuit. Consequently, the number die that can be put a wafer is a direct determinant of the sales that a wafer fab can achieve. This why the term 'Silicon Real Estate' is commonly used by industry veterans.

The following example illustrates why silicon real estate is so critical:

> A six inch wafer contains nine times more silicon surface area than a two inch wafer. A 256K RAM die typically has an area of some 35,300 square mils. A two inch wafer could hold as many as 80 such die. A six inch wafer could hold as many as 727 of the same size die. At recent selling prices of $10.00, and yields of 60%, the semiconductor manufacturer can achieve revenues of $4362 from a six inch wafer, but only $480 from a two inch one.

The cost of manufacturing a wafer will only slightly increase with size as Figure 1.1.8.2-3 shows. This happens because the relative amount of resources needed to process a wafer is only loosely related to size. Manufacturing with six inch wafers returns substantial profits as opposed to losses that are incurred while manufacturing with two inch wafers. A semiconductor manufacturer will almost always opt for a larger wafer size. There is one exception to this rule: Most prudent manufacturers will be hesitant about switching to the latest wafer size. The technology for the latest wafer size is seldom fully developed. Developing a new generation of wafer sizes can be very expensive for a semiconductor company. Moreover, yields are lower while costs are higher for a new generation wafer size. Thus, net pretax profits are lower. A semiconductor manufacturer will typically buy equipment that is upgradeable to the largest wafers possible. However, it will actually process wafers that are one size smaller. Two advantages accrue as a result: First, it can readily expand to the larger wafer size when needed; second, yield will be higher, since equipment designed for larger wafers will have better uniformity on smaller wafers.

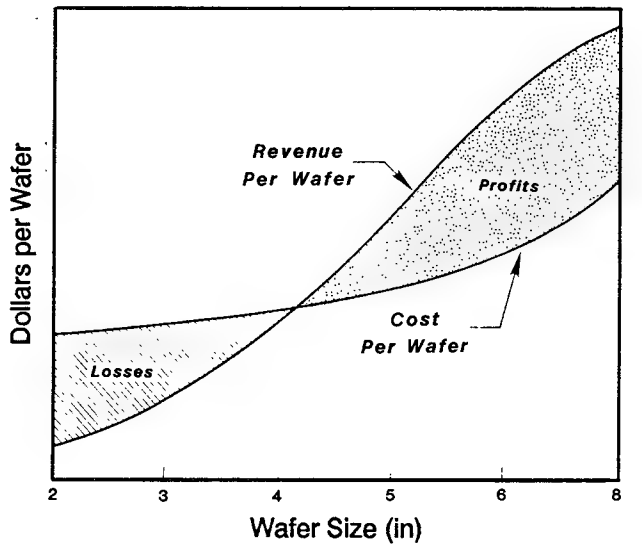


Figure 1.1.8.2-3

The Economics of Wafer Size
(for dynamic memories)

Nevertheless, the real pressure on a semiconductor manufacturer is still to reduce die size, for this improves both output quantity and yield. Linewidths are a critical determinant of die size. Total output of die will improve as the square of the reduction in linewidth. Moreover, yield will have an exponential effect on good die outs. All that typically is needed to accomplish a die shrink is a new mask design with finer linewidths. Together these improvements create major advantages to a semiconductor manufacturer. So its emphasis will be upon die size reductions first, and upon wafer size increases later. These factors have been a key driving force for semiconductor manufacturers since the beginning of the industry.

Figure 1.1.8.2-4 shows actual die size evolution for each generation of DRAM. An example of how reduction in die size increases quantity can be seen in the evolution of the 4K RAM. When the 4K RAM was first introduced in 1971, it was produced on a die that was roughly 40,000 square mils in area. By 1979 this circuit had undergone four mask design changes and had been reduced to about 12,000 square mils. But the product continued to be made on a three inch wafer. In return for that shrinkage, the same wafer size was producing 589 total die in 1979, versus 176 total die in 1971. This represented a 3.3 fold increase in output due to just die shrinkage alone.

Yield increases were equally dramatic. At the time, 40,000 square mil die would typically yield 20% net good die at wafer probe. A 12,000 square mil die would net about 60% good die. These combined advantages gave semiconductor manufacturers a 10 fold increase in output. And the only price paid was redesign and relayout of the die.

Die size reduction is still critical today. Die sizes have steadily increased throughout the eighties. It is not uncommon for sampling prototypes of new generation ULSI designs to be in excess of 110,000 square mils. Today initial yields for a new device generation can be below the 15 percent range. A die shrink to 88,000 square mils will improve yields to almost 25%. This will increase good die outs from 33 die per six inch wafer to 77 die per wafer. Consequently, a semiconductor manufacturer can expect to see similar improvements in quantity of output through linewidth reduction, as in the past.

One might ask, is there an upper bound on practical limits to die size? The answer is a qualified yes. But it is largely limited to the state-of-the-art of technology, more than it is to any fundamental limitations. The reason has to do with defect density and yield. Since yield is limited largely by die area. Die area is determined by linewidth and component count. Defect density is determined by the state of manufacturing technology. Most semiconductor manufacturers claim that the affordable yield limit for introducing a new product is 20%. At this value, a 90,000 square mil die will require a fab manufacturing capability that can support a defect density of 2 defects per square inch over 9 mask levels. Figure 1.1.8.2-5 shows that this level is currently the state-of-the-art for most American merchants. But if die size is increased to 190,000 square mils, (440 x 440 mils), yield drops to 3%. Defect density will largely determine the competitiveness of a semiconductor company. For example, a typical Japanese company could produce the same die with 11% yields, while an American captive producer could yield 43%. This is why American captive producers can economically produce devices that are one to two generations ahead of merchant producers.

This leads to the issue of packing density. Just how much can be packed in those chips? That will be dependent upon the size of the component (transistor, resistor or capacitor) put down on the die, as well as the linewidth in-between each die. With current technology, there are three practical limits to packing density. One is the width and the current carrying capacity of the metal stripes connecting each element. Another is the voltage that can be withstood by

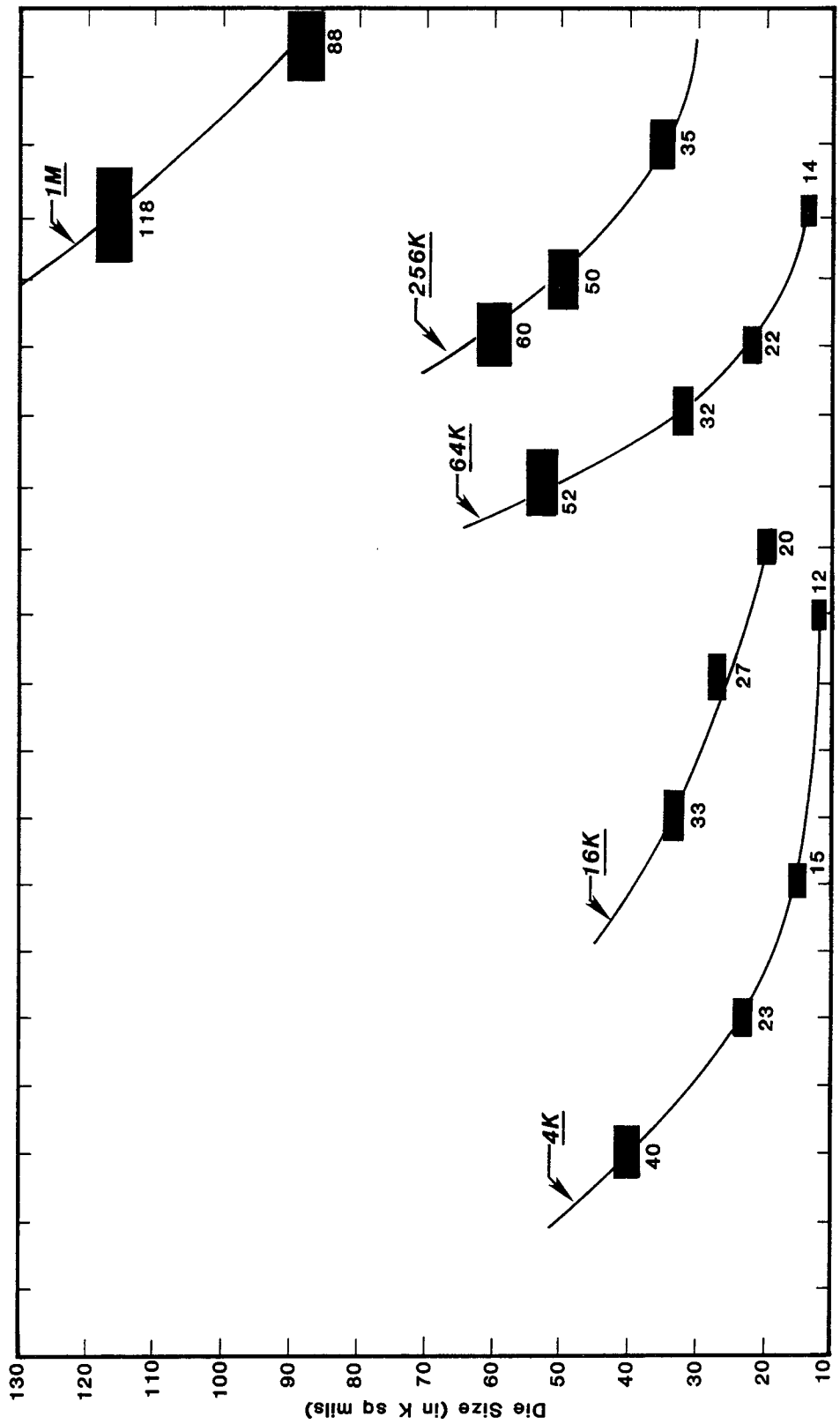


Figure 1.1.8.2-4

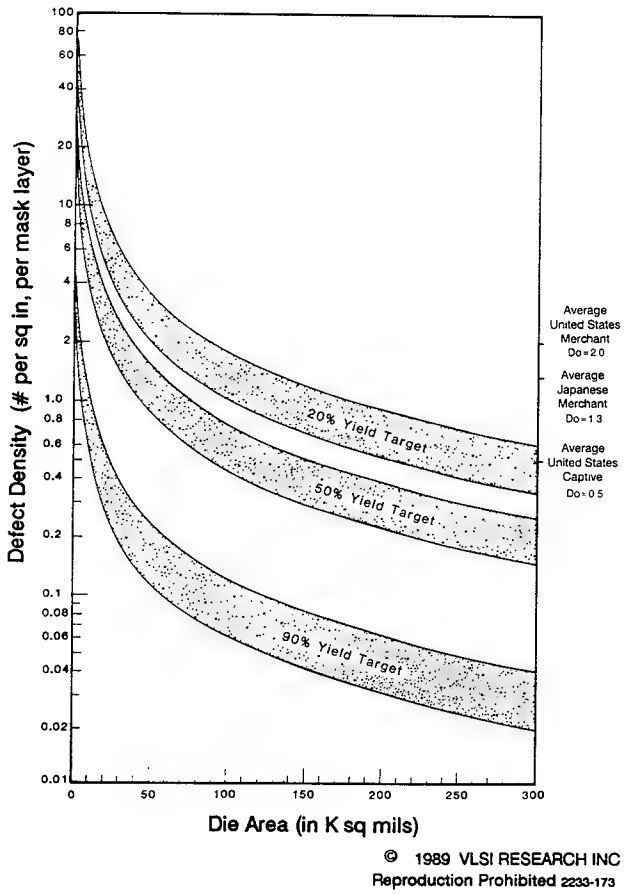


Figure 1.1.8.2-5

DEFECT DENSITY NEEDED TO ACHIEVE YIELD TARGETS

Uppermost portion of shaded areas represents 9 mask circuits, lower portion represents 16 mask circuits

each element. A third is the topographical layout limits that can be achieved with single layer, or with two layer, conducting surfaces. Transistors require three connections. In MOS transistors, one of these—the gate—will usually be fabricated of polysilicon on one conducting surface, while the other two—the source and the drain—will be fabricated of metal on another surface.

Source-drain connections to the transistor must have at least two stripes and two spaces at the optical limits. These will be equally spaced when maximum packing density is needed. Linewidth limits will thus dictate that the packing density cannot exceed 25% at the optical limit given that the voltage is scaled down as geometries fall below one micron. This is needed in order to prevent voltage breakdown. (Highly doped silicon can withstand 30 volts per micron. MOS designs using a 7.5 volt maximum and a 2.5 times safety factor will only require 0.7 microns separation.)

Figure 1.1.8.2-6 depicts the status of the semiconductor industry's capabilities today combining all of these characteristics. It gives the relationship of die size and linewidth to packing density. Several typical devices are superimposed on the figure. Current optical equipment limitations begin to dominate at line widths below 0.8 microns. Current manufacturing techniques limit defect densities to 0.5 per square inch

The Boundary of Conventional ULSI

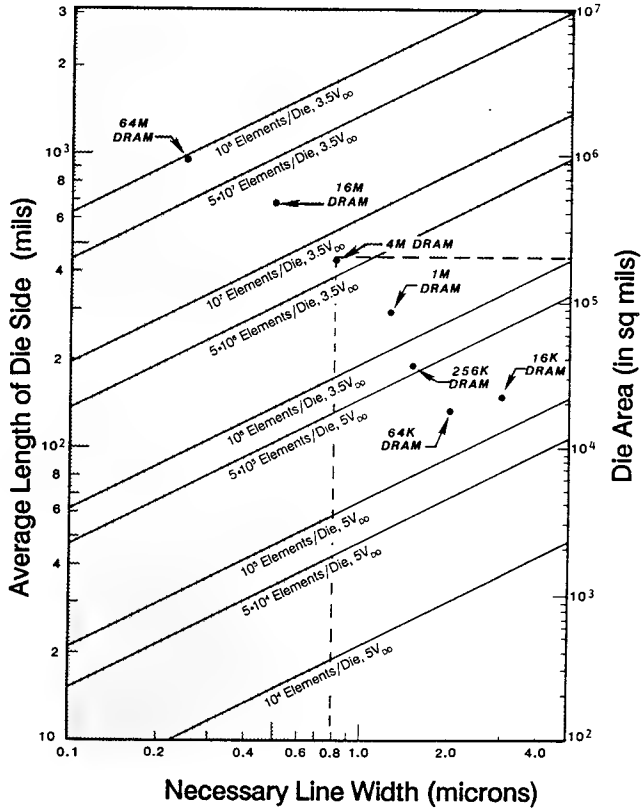


Figure 1.1.8.2-6

or above. Yield effects will become limiting at die sizes to about 200,000 square mils (447x447 mils per side) or smaller. These are the boundaries of today's optical and geometric capabilities.

In contrast, the boundary for LSI stood at linewidths of 1.5 microns. Production line defect densities of 4 per square inch limited to die sizes of 52,900 square mils (230x230 mils per side). It was VLSI equipment technology that made this progression from 1.5 microns to 0.8 microns possible.

It can be seen that the 4 Megabit DRAM is at the outer limits of current day manufacturing boundaries. These boundaries must be extended out in order for the industry to progress past the 4 Megabit DRAM. New technologies such as three dimensional scaling will be required.

For example, a 64 Megabit DRAM will require a planar surface area of almost one inch square even at three tenths of a micron linewidths! A defect density of 0.1 per square inch will be required. However, even if this can be accomplished, it will be extremely difficult to package such large die. Three dimensional scaling will be needed to reduce die sizes. However, this is not expected to alleviate the defect density requirement. This is because vertical scaling does not reduce actual surface area, it simply folds it, for more dense packing, like the folds in the human brain. Consequently, new generations of ultraclean production equipment will also be required.

Changes in materials will have a dramatic effect on equipment. Equipment can become obsolete overnight if materials requirements change. Electrical limitations force changes in materials as linewidths are reduced. Electrical scaling limitations arise from the physical phenomena which come into play as component sizes are reduced. There are three limits. One is the voltage breakdown of the material itself–as was mentioned earlier. The other is current density limitations. A third is the increasing sensitivity to alpha particles. All of these become pronounced when devices are manufactured in the 1 to 10 micron size region. Upon further shrinkage, the electrical parameters must be scaled.

Voltage breakdown is dependent upon two phenomena. One is the normal breakdown of the silicon material itself. The other is reduced breakdown due to very heavy doping. Pure silicon has a field breakdown limit of about 70 volts per micron. When stressed above this limit, the material will punch through. Silicon dioxide has a similar value of breakdown voltage. But with heavy doping, this is reduced to about 30 volts per micron.

Most digital devices manufactured today are designed for 5 volt operation. They typically have absolute maximum ratings of 7 volts. Manufacturers normally use a 2.5 times safety factor, bringing the maximum field voltage that can be safely applied to about 17.5 volts. With current day lithographic methods, this presents no major difficulty, devices will be separated by at least their optical linewidths. However, with deep UV and Eximer laser technologies, lower line widths become possible. Scaling to 3.5 volts has become necessary.

At a maximum linewidth of 0.4 micron, the maximum possible voltage which can be applied will be 12 volts. The actual operating voltage will probably be reduced to 3.5 volts maximum. It may possibly be reduced to a value as low as 3.0 volts.

Current handling limitations are also encountered. Alloys of aluminum, copper, and silicon are typically the conducting material. Metallization traces made from aluminum are normally about 5,000 Angstroms. The traces will also be about 1 micron wide. Consequently, the cross sectional area of an aluminum trace is now roughly equivalent to two times its linewidth. The fusing current of bulk aluminum is approximately 1.6 milliamperes per square micron. The fusing current of deposited aluminum is about 30 milliamperes per square micron for

metallized aluminum-copper-silicon in widths of the order of 1 to 10 microns.[†]

This is not normally a limitation. However, at these densities, electromigration of aluminum sets in. This reduces the practical values to about 1.5 milliamperes per square micron or about the same as bulk aluminum. This is a particular problem at oxide edges where the metal takes a sharp 90 degree bend. These current limitations have indirectly affected equipment manufacturers by generating pressure to use more sputtering and stimulating the need for aluminum etching equipment. Sputtering equipment has permitted the deposition of materials with better stoichiometry. This has reduced 'hot spots' where current peaking and burn-out can occur. Dry etching of aluminum mitigated undercutting of the aluminum. This reduced the number of 'pinched' metal areas and consequently also reduced 'hot spots'. These problems have continued well into the eighties further driving these markets.

Punch-through of aluminum contacts through shallow junctions into bulk silica has also become a problem. Barrier metals become necessary when junction depths fall below 250 angstroms. This has lead to demand for new selective tungsten CVD systems and reactively sputtered Titanuim Nitride films.

OPERATIONAL PARAMETERS

Operational Parameters will impact manufacturers in four main areas. They are:

- Operating Speed
- Pin Count
- Package Type
- Reliability

There has been continuous emphasis on greater device speed over the past three decades. Device speed is an important business driver. For semiconductor manufacturers, higher speed means value added to their products. This is true for both Very High Speed IC's (VHSIC's) and even low speed parts. Not every die on a wafer is the same. Operating speed can vary by as much as two times. The fastest parts can bring a ten to twenty percent price premium. Device speed is also an important business driver for both wafer fabrication equipment and questor systems suppliers. Process uniformity and low contamination levels in process equipment yields higher speed devices. Consequently, the value added through higher device speed drives demand for cleaner process equipment and inspection equipment. Speed is also an important driver of test equipment.
There are three areas where very high speed testing is of concern to users. One of these is with GaAs devices in military or aerospace applications. These are developmental devices that will generate demand for testing at speeds well beyond 100 MHz. They are just beginning to have a ready market as they come into production usage. Another issue is ECL testing. ECL testing will require test systems in the 50 to 100 MHz region. But ECL testing is a small market relative to overall digital testing requirements.

The other area where speed is of concern today is with emerging MOS memory and digital circuits. It has come to be generally accepted that bipolar devices are not particularly speed sensitive, but MOS devices are. MOS devices are much amenable to scaling because power densities are lower. Speed rises by the inverse of the reduction in linewidth. Moreover, device speeds in VLSI devices are interconnect limited. Consequently, transistor switching speed has little effect of overall device speed. These factors give MOS an advantage where both high speed and VLSI complexities are required.

[†] B. N. Agarwala, et al, "Width Dependence of Electromigration Life in Al-Cu, Al-Cu*si, and Ag conductors" 13th Annual reliability Symposium, 1975. IEEE Catalog #75CH0-931-6P4Y, PP 151-158.

Memory Cycle Time Versus Year Of Introduction

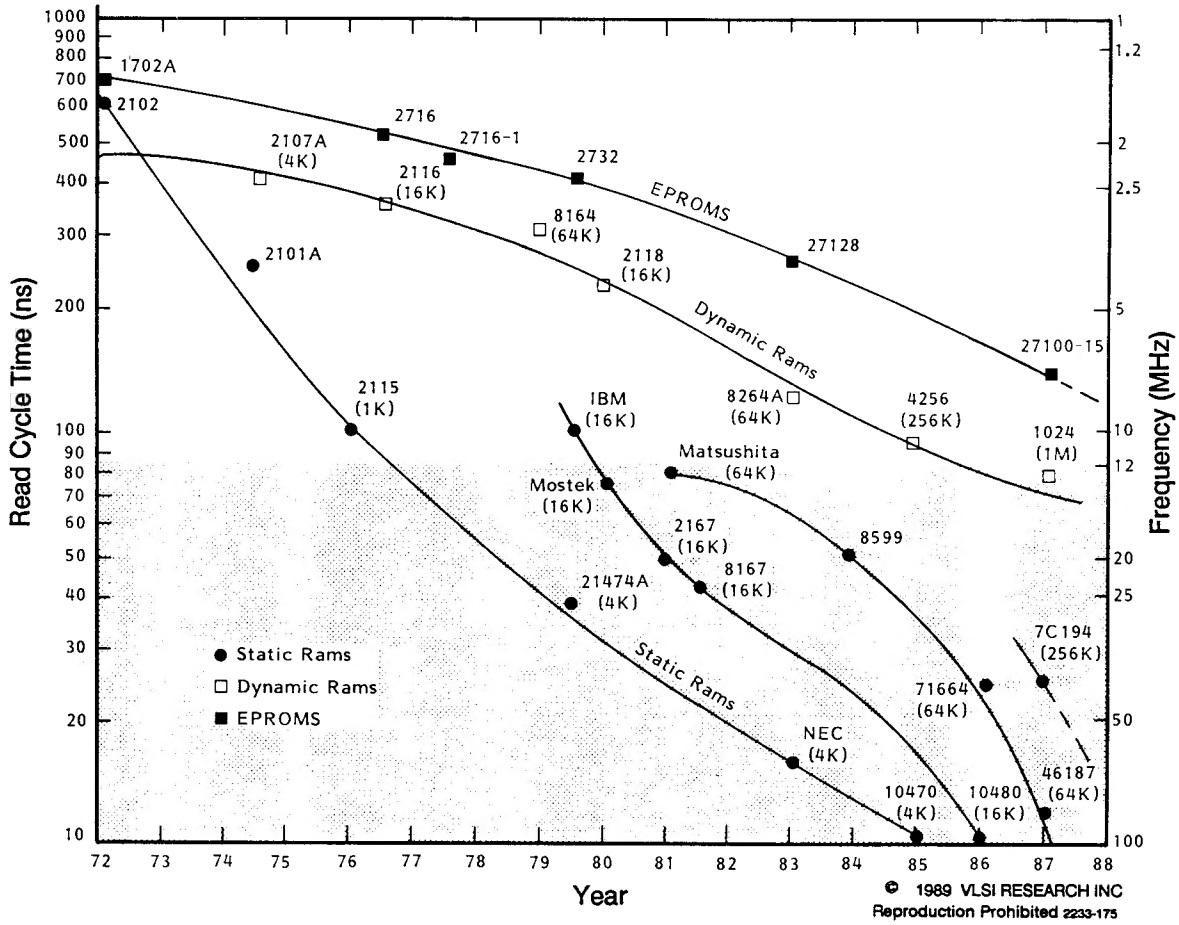


Figure 1.1.8.2-7

Speed gains in MOS memories have been well documented over the years. In recent years fast static RAM's have captured greater interest as CMOS static RAM's have approached the speed of bipolar units. Figure 1.1.8.2-7 demonstrates this. In this figure, the development of static RAM's, dynamic RAM's and PROM's is positioned as it has occurred over the years. Read cycle time is shown on the left ordinate. Equivalent frequency is shown on the right hand ordinate. The lightly shaded band shows the speed region of today's memory test systems. Almost all operate in the 12 to 40 MHz region. Some can even exceed 100 MHz.

Note from this chart that Dynamic RAM's and EPROM's are still exceptionally slow relative to today's testers. So speed will probably not become an issue with dynamic RAM's. Next, note the line of history of static RAM devices. The 4K static RAM has continued to pace the speed capability region of most of today's testers. But the newer 16K bit and 64K bit memories have also caught up with 4K bit ones. All three

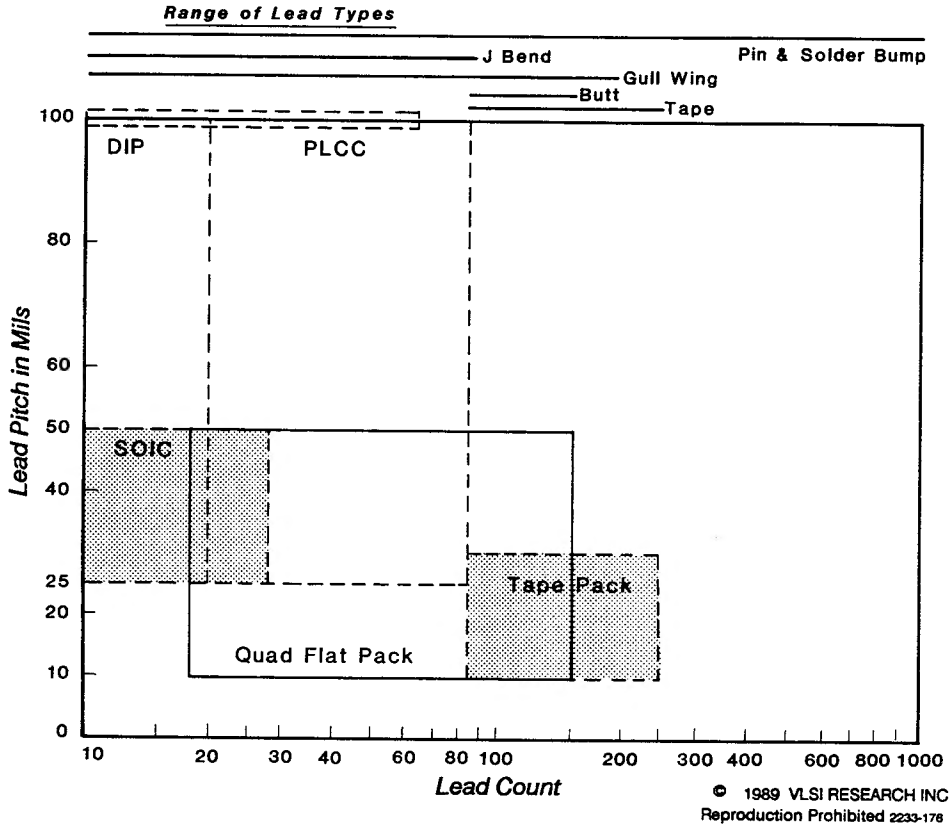


Figure 1.1.8.2-8

USABLE PACKAGE RANGES

operate at or close to 100 Mhz. Consequently, speed will continued to be an issue in Static RAM testing.

The advent of high density logic parts has served to drive pin counts up. For logic devices, pin counts rise as gate counts increase. One general rule of thumb that can be used is Rent's rule. It comes from IBM and is outlined in VLSI Electronics†. This rule shows that actual pin count rises just a little faster than the square root of gate count–about 2/3.

In the past, the pin counts issue was solved through multiplexing the inputs and outputs. Lowering pin counts through multiplexing lowered package costs. However, the advent of ASIC devices shifted cost centers from packaging to design. Designs costs are a significant portion of an ASIC devices' total costs. This is because production volumes are so low for ASIC's. Design complexity must be kept to minimum in order to reduce its costs.

Once a design has been completed, reducing the design's pin count increases costs. Such constraints are costly since design time is increased when designers have to add circuitry to multiplex outputs. The pressure on designers has been to reduce design time, not increase them!

Consequently, pin counts have edged up in recent years. Most gate arrays with gate counts of 10K or above have in excess of

† VLSI Electronics, Vol. I, Academic Press Inc., 1981, pp 203-204.

200 pins. Fujitsu's 100K gate array has 400 pins. This trend has affected test equipment the most. It has also had a significant impact on packaging. As pin counts rise, lead pitch falls and package shape becomes square. This drives semiconductor manufacturers into new SMT (Surface Mount Technology) package styles. The advantage to the semiconductor user is greater board stuffing potential.

The effect on packaging is shown in Figure 1.1.8.2-8. It gives the usable lead count ranges of the various package styles versus their lead pitches. Pin Grid Arrays (PGA's) and solder bumping push the limits out beyond a thousand pins. However, PGA's are very costly in comparison to most SMT packages. The combination of lower cost and greater value added drives semiconductor producers to SMT package styles with finer lead pitches. SOIC's and PLCC's already satisfy most needs. Quad flat packs extend the limit of PLCC's from 84 leads toa minimum of 134. Many manufacturers believe that they are even extendable to 150 leads. Tape pack extends the limit to 256 leads. Each of these new packages will drive demand for new types of handlers and assembly equipment.

Product reliability is becoming an increasingly important business driver for semiconductor manufacturers. Angelo Rapa of IBM recently stated that reliability was becoming equally as important as yield to a semiconductor manufacturer. The cost of field repair far outweighs the actual cost of a device. Moreover, semiconductor customers want to avoid the cost of incoming inspection. The need for control over reliability drives semiconductor producers to seek better process control and process stability. This in turn drives demand for better wafer process equipment and questor systems.